

# Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

**COMPLETE, LOW-DISTORTION IC MIXER FOR FREQUENCIES UP TO 500 MHz (page 3)**

More about sigma-delta converters and their applications (see pages 6 & 24)

Audio preamplifier circuits for microphones (page 12)

Complete contents on page 3





# Editor's Notes

## NEW FELLOWS

We are pleased to note that Richie Payne and Paul Ruggerio were introduced as Analog Devices Fellows at our 1984 General Technical Conference. *Fellow*, at Analog Devices, represents the highest level of advancement that a technical contributor can achieve, on a par with Vice President. The criteria for promotion to Fellow are very demanding. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art; their significant technical contributions will have had a major impact on the company's revenues; they must have demonstrated superior creative ability in product- or process technology leading to commercial success.

Other attributes include roles as mentor, consultant, organizational bridge, gatekeeper, entrepreneur, teacher, and ambassador. They must also be effective as leaders of teams and contributors to team effort and in understanding the needs of the customer. Our two new Fellows' accomplishments and technical abilities, as well as their personal qualities, well-qualify them for this appointment. They join Fellows Derek Bowers (1991), Paul Brokaw (1980), Lew Counts (1984), Barrie Gilbert (1980), Jody Lapham (1988), Fred Mapplebeck (1989), Jack Memishian (1980), Mohammad Nasser (1993), Wyn Palmer (1991), Carl Roberts (1992), Brad Scharf (1993), Mike Timko (1982), Bob Tsang (1988), Mike Tuthill (1988), and Jim Wilson (1993).



## PAUL RUGGERIO

Paul Ruggerio has been a key contributor to Analog Devices semiconductor manufacturing, in ways too numerous to mention, from the day we acquired our first fab in the early '70's. His expertise embraces the broad areas of lithography, thin film, IC passivation, and metallization. His early contributions include our first Epi facility, maskmaking, projection aligning, chrome masking, and stepper lithography. He was one of the industry's first investigators in the area of ultraviolet resist stabilization.



His supporting role in innovative photomask technology made possible the first complete single-chip A/D converter, the AD571 (*Analog Dialogue* 12-1, 1978). Later, he led a team that developed the universal double-level metallization process, now widely used within Analog Devices. Thin-film precision resistors have been a key to ADI's preeminence in high-performance analog ICs; Paul has studied the chemistry, composition, and structure of thin-film materials and has invented masking schemes and optimized target compositions to obtain thin-film resistors with desired properties.

Graduating in 1963 from Rochester Institute of Technology, with a BS in Photographic Science and Engineering, Paul joined the GTE Development Laboratory in Bayside, NY, working in the new field of photolithography and mask-making for semiconductor manufacturing. After 5 years, he went to work at Sprague Electronics, in maskmaking and IC process development. He joined Analog Devices in 1973.

 Dan Sheingold

## RICHIE PAYNE

Dr. Richard Payne is best-known in recent years as leader of the team that developed the prize-winning ADXL50 accelerometer, which brought surface-micro-machining to commercial viability. However, he has a long career of technical contributions to semiconductor processing, going back to the '70's, when he did pioneering work at Bell Labs, inventing the first successful process for fabricating high-frequency bipolar transistors using ion implantation.



At Analog Devices, he has contributed to and managed process development for high-performance linear, digital, and mixed-signal devices. The strategies and people that he put in place have significantly enhanced Analog's leadership position in high-performance analog and mixed-signal technology. He also built and managed a major wafer-fabrication facility that put the results of process development to the severest test: the ability to manufacture and ship advanced ICs in significant quantity.

He has an A.B. degree from Dartmouth and received his Ph.D. in Physics from Yale in 1970. He is a Fellow of IEEE; in 1992, he received the IEEE Electron Device Society's J.J. Ebers Award for "engineering achievements in process architecture and device design for twin-tub CMOS integrated-circuit technology, contributions to bipolar technology, and advancement of these technologies in commercial utilization."

## THE AUTHORS

**Rupert Baines** (page 8) is a Senior Technical Marketing Engineer in Corporate Marketing, where he specializes in IC products for Communications. He has a BSEE from the University of Hull (United Kingdom) and an MBA from IESE in Barcelona (Spain). Hobbies include socializing, travelling, and crashing jet-skis.



**Mike Curtin** (pp. 6-7) is a Senior Applications Engineer at our Limerick, Ireland, facility. His photo, and a biographical sketch, appeared in *Analog Dialogue* 27-1, 1993.

(More authors on page 30)

**Cover:** The cover illustration was designed and executed by Shelley Miles, of *Design Encounters*, Hingham MA.

## Analog Dialogue

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# Low-Distortion Mixer: +24 dBm 3rd-Order Intercept for Only -10 dBm LO Power

**500-MHz AD831 integrates a doubly balanced mixer, LO preamplifier, and output amplifier, all in a 20-pin PLCC**

by Bob Clarke and Barrie Gilbert

The AD831\* is a wide-dynamic-range monolithic mixer designed for use in demanding applications. Its low distortion features a +24-dBm third-order intercept point ( $IP_3$ ). In addition to the basic mixer circuit, it includes an output amplifier and a local-oscillator (LO) input amplifier (Figure 1). The LO input amplifier is a limiting preamplifier, requiring only -10 dBm of local-oscillator drive. RF and LO frequencies up to 500 MHz can be used; at 500 MHz, the third-order intercept exceeds +20 dBm. To simplify impedance matching, both the RF and LO ports provide differential high-impedance inputs that can be ac or dc coupled and driven from either differential or single-ended sources.

The AD831's low-distortion IF amplifier provides a low-impedance output voltage suitable for driving reverse-terminated filters. The gain of this amplifier, and thus the conversion gain of the mixer, can be increased using external resistors.

The AD831 supplants diode-ring or FET-ring mixers, which could require as much as 1 watt of LO power for high-intercept performance. Such mixers require an external LO preamplifier to generate sufficient drive to switch the diodes or FETs into hard limiting—and shielding to minimize electromagnetic interference (EMI) from the high-level LO. An output diplexer may also be needed for proper 50-ohm termination.

The AD831, shown in simplified detail in Figure 2, comprises three functional blocks: a mixer, a LO preamplifier, and an output amplifier. The mixer is a doubly balanced Gilbert multiplier circuit, supported by a very linear, low-noise V/I converter at the RF port,

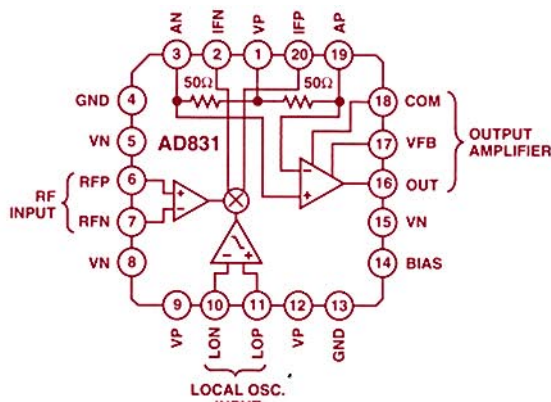
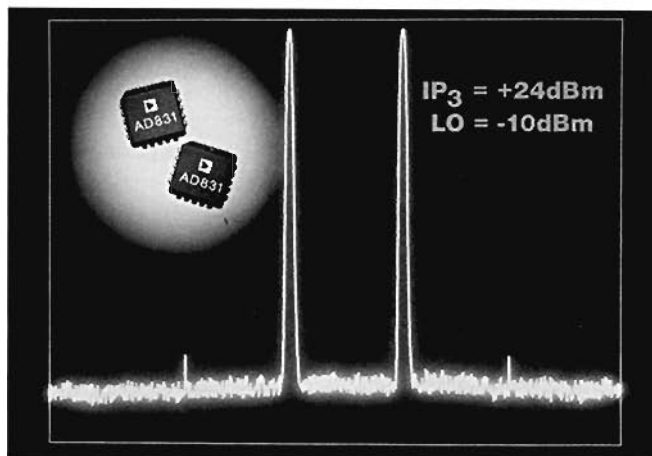


Figure 1. The AD831 consists of a mixer, LO preamplifier, and output amplifier in a 20-pin PLCC.

\*For technical data, use the reply card. Circle 1



and a high-gain, high-speed driver stage in the LO path. In the mixer core, the RF signal is multiplied by a square wave at the LO frequency. For sinusoidal RF signals, the mixer produces the sum and difference frequencies, plus a series of higher harmonics. Since the output will be filtered to remove all but the sum or difference frequency, and only half the signal power appears in each, it would suffer a loss of about 6 dB. However, the amplitude of the fundamental in the multiplying square wave is  $4/\pi$  (i.e., 2.1 dB). Thus the net conversion loss is only 3.9 dB; the AD831's output amplifier provides the gain required to restore the overall conversion gain to 0 dB.

The LO preamplifier is a high-gain limiting amplifier; it accepts a low-amplitude input, which may be either sinusoidal or square-wave—and converts it into a balanced square-wave output that drives the mixer core. The amplitude of a sine LO input can be reduced to -20 dBm (an amplitude of 32 mV) at local oscillator frequencies below 100 MHz, and to -10 dBm (100 mV) at 500 MHz, without substantially reducing conversion efficiency.

The IF output from the mixer core is available as either a differential low-level output at pins IFN and IFP, or as a single-ended high-level voltage output at pin OUT. The differential outputs at IFN and IFP are from nominal 50- $\Omega$  source impedances, and they provide the full 500-MHz output bandwidth when ac-coupled to a load via a transformer or capacitors. In down-conversion (difference-frequency) applications, a single capacitor connected between these terminals can implement a low-pass filter to reduce

## IN THIS ISSUE

Volume 28, Number 2, 1994, 32 Pages

Editor's Notes (New Fellows: Richie Payne & Paul Ruggiero), Authors	2
Complete, low-distortion mixer for frequencies up to 500 MHz (AD831)	3
Instrumentation Applications of the New $\Sigma$ - $\Delta$ Converters (AD7714 & 7716)	6
GSM chip set implements all baseband functions (AD20msp410)	8
Two new LVDT interface ICs with analog or digital output (AD2S93, AD698)	9
Serial-input 16-bit current-loop DAC has choice of ranges (AD420)	10
800-MHz op amp has high performance, low power, low cost (AD8001)	11
Microphone preamplifiers for audio—a brief guide for users	12
New-Product Briefs:	
What's new in A/D converters, multiplexers, codecs	19
What's new in D/A converters, analog switches	20
What's new in op amps and analog multipliers	21
What's new in interfaces, regulators, and temperature sensors	22
A reader notes—Comments on high-frequency signal contamination	23
Ask The Applications Engineer—16: Using Sigma-Delta converters, part II	24
Worth Reading, Authors	30
Potpourri	31



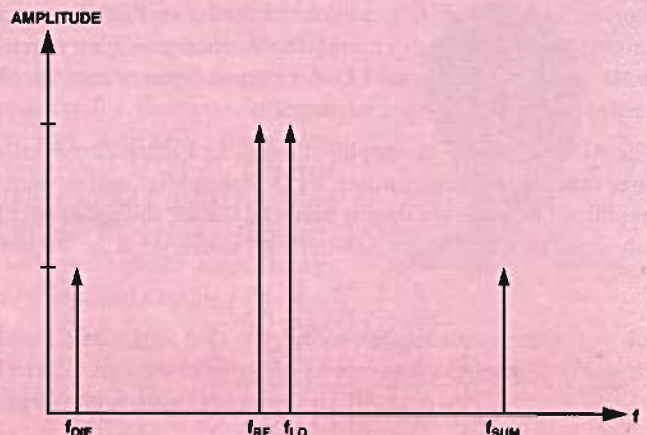
## ABOUT MIXERS

No one active in "RF-land" needs to be told what a "mixer" is or of its pivotal importance in determining the overall performance of an RF circuit, especially a receiver. However, a brief discussion of what mixers do, a couple of popular approaches, and some of the terminology will be helpful to readers who specialize in other disciplines but have a healthy curiosity about this ubiquitous function for which analog circuits are still of vital importance.

A mixer, as defined in the *Dictionary of Electronics*, by S. W. Amos, (Butterworths, 2nd edition, 1987), is "a device which accepts two inputs at different frequencies and generates an output at the combination frequencies. In particular, the RF mixer in a superheterodyne receiver accepts an input from the antenna (or an RF amplifier) and from the local oscillator and generates an output at the sum or difference frequency which is equal to the intermediate frequency."

A mixer is a member of the class of nonlinear elements used for frequency translation. The most productive of these elements form a subclass sharing the property of signal multiplication—in one way or another their output is the product of two inputs. For example, an *analog multiplier*—such as the Analog Devices AD834—produces an output precisely proportional to the instant-by-instant product of its two inputs.

If the two inputs are ac sinusoids at frequencies  $f_{RF}$  and  $f_{LO}$ , a trigonometric identity shows that their product will contain two sinusoids, at frequencies  $f_{RF} + f_{LO}$ , and  $f_{RF} - f_{LO}$ , with amplitudes equal to one-half the product of their individual amplitudes. For example, if  $f_{RF} = 1.5$  MHz and  $f_{LO} = 1.955$  MHz, the sum and difference frequencies will be 3.455 MHz and 455 kHz. A bandpass filter selects the signal at the desired frequency, for example, the AM broadcast band's 455-kHz intermediate frequency (IF).



In general, the RF signal will not be a simple sinusoid; it will represent the sum of sinusoids having a range of frequencies in the neighborhood of a carrier,  $f_{RF0}$ —for example,  $1.5$  MHz  $\pm$  10 kHz. Each frequency term, when multiplied by the  $f_{LO}$  term, will produce sum-and-difference terms; the result will be two bands of frequencies at  $3.455 \pm 0.01$  MHz and  $455 \pm 10$  kHz. Again, a bandpass filter can be used to select the desired frequency band. Note that if  $f_{LO}$  is equal to the carrier,  $f_{RF0}$ , the sum term will be centered at twice the carrier

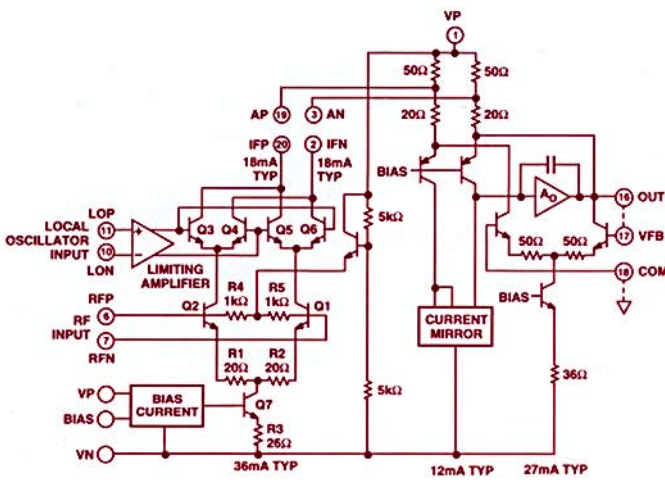


Figure 2. Simplified schematic of the AD831

the amplitudes of the unwanted sum component, for decreased intermodulation in the IF amplifier.

The gain of the AD831's output amplifier can be programmed using a pair of feedback resistors placed between the pins OUT, VFB, and COM. When OUT is tied directly to VFB, the small-signal bandwidth, using the amplifier, exceeds 250 MHz. The amplifier's low dc offset allows it to be direct coupled in such applications, and in some cases the AD831 may be used in direct-to-baseband applications.

## APPLICATIONS

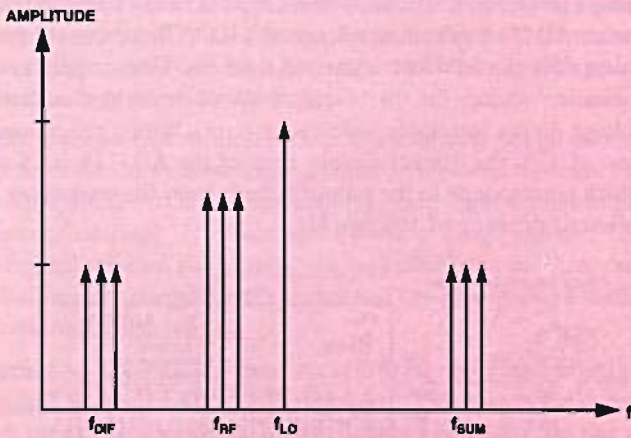
The AD831, with its low distortion and wide dynamic range, provides an ideal solution in receivers for multi-signal environments, in which the mixer must cope with an abundance of high-level desired and undesired inputs. In RF modems, two AD831s can be used to make a quadrature (IQ) modulator or demodulator. The -10-dB LO drive requirement and high input impedance allows the AD831 to be driven from passive phase shifters or digital phase shifters constructed from ECL gates, with the additional advantage that small LO inputs minimize the risk of feedthrough and EMI.

Since the AD831 is dc-coupled throughout, it can be used as a modulator. In a suppressed-carrier application, the carrier is applied to the LO port and the modulation signal is applied to the RF port. The nominal full-scale signal level at the RF input is  $\pm 1$  V (+10 dBm), but some overrange can be tolerated. As a simple amplitude modulator (AM), a baseband signal of 0-to-1 V applied to one of the RF inputs controls the RF output. In these applications, the built-in gain of the output amplifier will result in 3.9-dB more gain than in the mixing mode.

The AD831 is the newest of a growing family of linear parts for RF and IF applications from Analog Devices. Others include the AD600, AD602, and AD603 amplifiers for low-noise linear-in-dB gain control, the AD734 and AD834 linear multipliers, the AD640 precision wideband log amp, and the AD606 logarithmic/limiting amplifier that provides both hard-limited IF and received-signal-strength-indicator (RSSI) outputs.

The AD831 requires  $\pm 5$ -volt supplies or a 9-to-11-volt single supply, drawing 125 mA maximum (programmable) quiescent current. Housed in a 20-lead PLCC, it operates over a supply range of -40 to +85°C. An evaluation board is available. Pricing in 1000s is \$12.

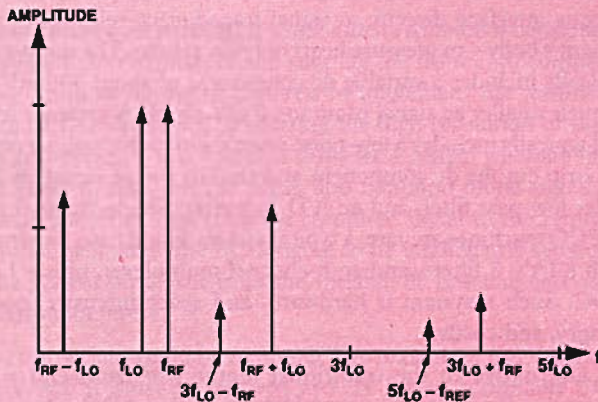




frequency and the difference term will reproduce the  $\pm 10$ -kHz baseband signal associated with the carrier.

Multiplication by a sinusoidal LO signal produces a fairly simple frequency spectrum, but the output amplitude (signal gain) is sensitive to the amplitude of the LO. For better precision, modulators that amplify and clip the LO signal—such as the AD831—are used to set the amplitude of the output (IF signal) to a value that is proportional only to the RF signal. However, the spectrum of a clipped waveform (square wave) contains a family of odd harmonics of  $f_{LO}$ ; therefore, the multiplication produces the sum and difference of each of these harmonic components with each frequency present in the RF signal. Although they will be suppressed if the difference signal is chosen, the large number of frequencies present requires a highly linear operation, because nonlinearities can produce additional harmonics and cause intermodulation products to appear in the difference band.

Key objectives in the design of a high-performance active mixer are to achieve a very linear RF input section, followed by a near-ideal polarity-switching stage, followed by a very linear IF output amplifier prior to the first filter.

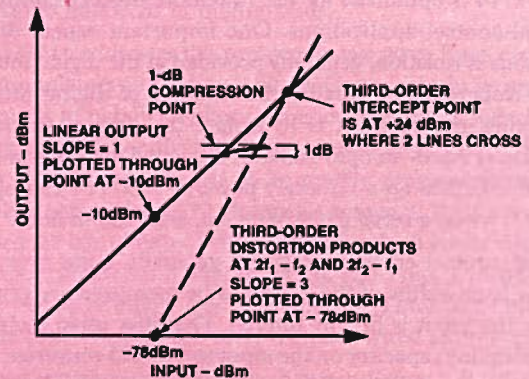


### MIXER TERMINOLOGY

**Intermodulation distortion:** If the input to an ideally linear circuit is a pair of sinusoids at frequencies  $f_1$  and  $f_2$ , the output will contain only those frequencies. The output of a circuit with nonlinear distortion, viewed with a spectrum analyzer, can contain such frequencies as  $2f_1$  and  $2f_2$  (second harmonic distortion),  $3f_1$  and  $3f_2$  (third harmonics), etc., as well as

$f_1 + f_2$  and  $|f_1 - f_2|$  (second-order intermodulation products),  $|f_1 + 2f_2|$ ,  $|f_1 - 2f_2|$ ,  $|2f_1 + f_2|$ , and  $|2f_1 - f_2|$  (third order intermodulation), and so on. An ideal mixer's output will contain only those frequencies that are expected according to theory. A mixer with distortion will also contain harmonics and intermodulation-products of input and output frequencies. For small signals, distortion is generally negligible, but as the amplitude approaches saturation, distortion products increase rapidly.

**Third-order intercept point:** A frequently used figure of merit for device linearity. The third-order intermodulation difference products ( $f_1 - 2f_2$  and  $2f_1 - f_2$ ) are those most likely to interfere with the desired signals. If device output power (unity slope) and third-order intermodulation (slope of 3) are both plotted against input power on a logarithmic scale, and the plots are then extrapolated until the two functions meet, the output power (dBm) at which the intersection occurs is called the *third-order intercept point*. The larger this number, the better the device's overall linearity is presumed to be. The analysis on which this criterion is based assumes that distortion for a particular device can be modeled with a power-series expansion.\*



**Diode-ring mixer:** A commonly used mixer topology for many years, employing a ring of four diodes, driven across one diagonal from the local oscillator, and across the other from the RF input. Both sources are transformer coupled, and the output is taken between the center taps of the transformer secondaries. The diodes may be silicon junction, silicon Schottky barrier, or gallium arsenide types. A major disadvantage of this circuit is the need for high drive power at the LO input, in order to ensure that the diode conduction is strong enough to achieve low noise and to allow large signals to be converted without excessive spurious nonlinearity. Other disadvantages include difficulty in impedance matching, coupling between ports, and insertion loss of this *passive* circuit.

**1-dB gain compression:** The level of input power at which the output drops to 1 dB below the theoretical value—the “knee” of the output-input plot (see above figure).

**Conversion gain:** The gain from the RF port to the IF port. Usually  $< 0$  dB for passive mixers. Active mixers, such as the AD831, provide higher conversion gain (nominally 0 dB, but adjustable by choice of external resistors) and better port-to-port isolation.

\*For a fuller explanation, see *Analog Dialogue* 27-1 (1993), “Ask the Applications Engineer—13: Amplifier distortion specs”, by Walt Kester, pp. 27-29.



# Instrumentation Applications of New Sigma-Delta A/D Converters

## Single-supply, low-power 24-bit A/D converter digitizes low-level signals in industrial-control applications

Mike Byrne

The AD7714 is the newest member of the AD771x family of 24-bit sigma-delta converters (*Analog Dialogue* 26-1, pp. 7-9). Like other members of this high-resolution family, the part provides a programmable-gain front end and a programmable digital filter. It features very low noise (<300 nV rms at a gain of 128) and an input channel arrangement that accepts 3 fully differential—or 5 pseudo-differential—inputs.

The AD7714 is optimized for use in remote process-control and industrial-control applications. One important aspect of such applications is isolation, generally provided at the digital interface by opto-isolators. The smaller the number of digital interface connections, the easier it is to isolate the device, since each connection requires an opto-isolator. Designed with this in mind, the serial interface on a remotely powered AD7714 can operate with just 3 wires: a serial clock, *data out*, and *data in* lines.

Industrial control environments are generally quite noisy and, since, the bandwidths of the signals to be measured are generally very low, the input is heavily filtered. The filter often includes a large decoupling capacitor on the input to the A/D converter. Since the input to an unbuffered sigma delta converter is effectively a sampled capacitor system, source impedance associated with decoupling capacitors results in a gain error. The AD7714 on-chip buffer avoids this problem.

Power requirements are also of concern. In many cases, the power to the remote transducer site is provided to devices in series in a 4-20-mA analog data loop. In such applications, devices in the transducer circuit must be able to operate on less than 4 mA. In other cases, with isolated digital outputs, remote power may be furnished by batteries. Meeting both of these low-power requirements, the AD7714 can operate from a 3-V power supply, consuming only 500  $\mu$ A of supply current. In its power-down mode, standby current is typically less than 10  $\mu$ A.

The programmable-gain front-end on the AD7714 allows it to handle unipolar analog inputs with ranges from 0 to +20 mV to 0 to +2.5 V and bipolar inputs of  $\pm 20$  mV to  $\pm 2.5$  V. Because the part operates from a single supply, the differential bipolar ranges are centered about an offset common-mode input.

Figure 1 shows the analog connections for a typical application of the AD7714 in pressure measurement, reading the differential output voltage from a Sensym BP01 pressure transducer. With rated full-scale pressure (in this case 300 mm Hg) on the transducer, the full-scale differential output voltage from the bridge is 3 mV for each volt of excitation, or 15 mV with a 5-V supply. The reference voltage is derived from the 5-V excitation voltage,

using a divider with resistance values of 24 k $\Omega$  and 15 k $\Omega$ , as shown, for an AD7714 reference voltage of 1.92 V. Since the reference voltage for the AD7714 is derived from the same supply as the excitation voltage for the bridge, drifts of the bridge excitation voltage do not introduce scale-factor errors. With a programmed gain of 128, the full scale input span of the AD7714 is 15 mV, which corresponds to the output voltage from the transducer for full-scale pressure of 300 mm Hg.

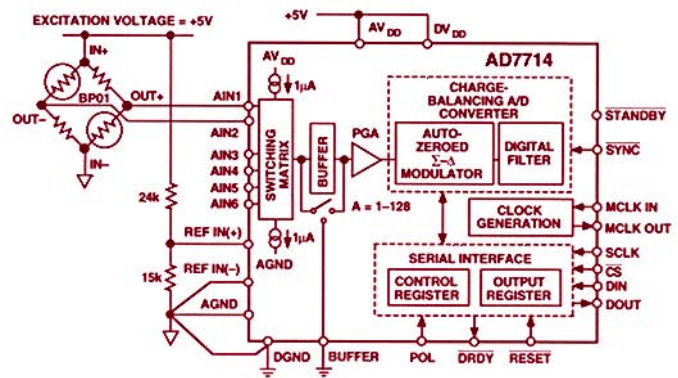


Figure 1. Pressure measurement using the AD7714.

The AD7714 is housed in 24-pin plastic & hermetic DIPs & SOICs and 28-pin SSOPs and is available for the -40 to +85°C and -55 to +125°C temperature ranges. Prices start at \$13 (100s).

*The AD7714 was designed at the Analog Devices facility in Limerick, Ireland, by a team led by Pat Hickey.*

## Sigma-delta techniques reduce hardware count and power consumption in biomedical analog front ends

Mike Curtin

Electrocardiograph (ECG) and electroencephalograph (EEG) equipment- and system designers have traditionally needed hardware-intensive input signal conditioning. The front-end circuits interface directly to signal transducers—electrodes on a patient's body—to measure heart or brain activity. The input signal typically includes a variable dc component of about 300 mV and a much smaller ac signal of up to 10 mV pk-pk. A system's front-end typically includes a low-noise instrumentation amplifier circuit (to strip out the dc component and amplify the ac signal), a 2nd-order low-pass filter, and an A/D converter. Single-channel EEG or ECG machines are rare; a typical system would have 8 channels, with 8 IA's, 8 filters, and an 8-channel multiplexer, plus a 12-bit ADC. Such a system is hardware- and space-intensive, power-hungry, and costly.

An alternative to the traditional method of front-end signal processing is to use a low-cost, high-resolution ADC (about 5 or 6 extra bits) to digitize the entire signal, including the variable offset. Then use the power of digital processing to extract the relevant information. For such an approach, the sigma delta conversion technique is very suitable.

- The wide dynamic range and low noise performance of the sigma delta converter obviate the need for a high-performance instrumentation amplifier.
- The analog low-pass filter can be reduced to simple anti-alias filtering for a sigma delta converter with suitable filtering.

• It is much easier to achieve a low-power front-end using sigma-delta converters. Typical power consumption is much lower than for traditional ADCs. This is very important for front-ends which operate from an isolated supply.

Some aspects of biomedical measurement-system design present problems similar to those found in industrial/process control. For example, ECG machines measure very small input signals in the presence of large dc offset and common mode signals. The traditional solution has been to use expensive front-end circuitry including instrumentation amplifiers and low-pass analog filtering to condition these inputs.

In addition, the ECG machine must process many channels. The standard 12-lead ECG requires various combinations of the signals from nine electrodes on the patient's body. The traditional way of doing this has been to compute the differentials between electrodes by means of hardware, as shown in Figure 2: this requires a set of differential amplifiers in the front end.

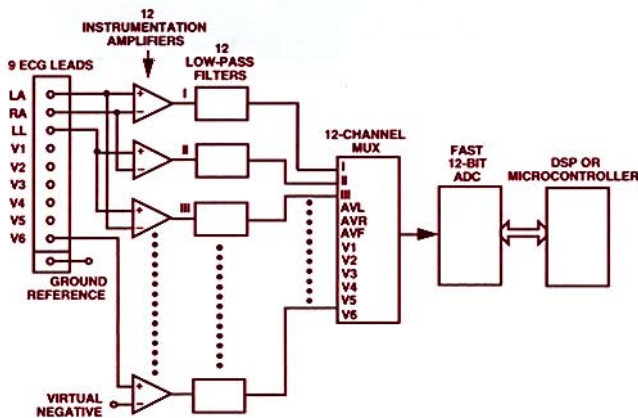


Figure 2. Conventional 12-lead ECG system.

The net result is a system that is hardware-intensive, expensive, and relatively inflexible. In a new approach, employing sigma-delta techniques, the AD7716\*, described here, was created to satisfy the specific needs of ECG system design.

**Resolution requirements:** If a sigma-delta solution is considered, it is possible to reconfigure and simplify the front end, compared to the depth of hardware required to implement the traditional 12-lead ECG. However, by utilizing the high resolution of sigma delta converters, it is possible to consider a system whereby there is no need to take out the offset and common-mode signals in hardware. Instead, digitizing the complete signal to the required resolution will allow the ECG signal to be intelligently separated by the system processor from the variable dc baseline and other normal-mode noise.

What resolution would be required? The maximum ECG signal is 10 mV, and it must be resolved to 5  $\mu$ V for an acceptable ECG plot. The typical offset voltage is 300 mV and so is the typical common mode voltage. Thus the total dc component could exceed 600 mV. Resolving a 600-mV signal to within 5  $\mu$ V—a ratio of 120,000—requires a converter with a usable dynamic range corresponding to 17 bits. This is easily possible with sigma-delta techniques; the AD7716 fulfills this requirement.

**Bandwidth requirements:** The bandwidth requirements for ECG machines depend on the application. There are two broad categories: diagnostic and monitor. The toughest requirement is for diagnostic systems, used in patient analysis and diagnosis. The

American Heart Association standard requires that a diagnostic ECG have a flat 0.14 to 50 Hz frequency response, with maximum attenuation of 3 dB at 0.05 and 100 Hz.

The bandwidth requirements are not as strict for monitors. Here, accuracy to within a few dB in the 5-25-Hz band is sufficient. Reduced bandwidth helps the monitors resist disturbances caused by electrical noise, body movements etc., but it also restricts the amount of information in the ECG. Manufacturers choose the bandwidth to meet specific requirements for their machines, often a compromise between diagnostic and monitor standards.

The AD7716 flexibly permits adjustment of the digital filter high-frequency cut-off, from 584 Hz to 36 Hz in binary steps. More-precise frequency setting, if needed, can be achieved by adjusting the device clock, since the cutoff frequencies scale in proportion.

**Easing multi-channel applications:** The number of ECG channels can range from three electrodes, in the most basic ECG machine, to systems which convert signals from more than 16 inputs. The AD7716 solution simplifies assembly of a multi-channel system. Traditionally, designers use a multiplexer and fast ADC to deal with multiple inputs. However, multiplexing sigma-delta converters is not practical; each time a channel is switched, the next conversion must wait for the digital filter to settle. This can require hundreds of milliseconds.

The AD7716 addresses this problem in two ways. First, each device has 4 modulators and 4 digital filters. Consequently, it can convert 4 channels in parallel without experiencing any sequential filter-settling delay. Secondly, the device interface's CASCADE facility allows a number of devices to be readily ganged together. Each channel's conversion ( $\leq 32$  channels) comes in the form of a 32-bit word: 22 bits of data, 2 bits to identify which one of the device's four input channels is being converted, and 3 bits to identify which device—of up to eight—has been selected. These three bits can be directly controlled by the user, via hand-wired address pins.

A typical system configuration is shown in Figure 3. It will consume less power, occupy less space and cost less per-channel than the conventional configuration of Figure 2. It also allows the designer more flexibility, because more of the system properties are accessible to software; in many cases, system performance can be upgraded without changing the hardware.

The AD7716 is housed in 44-pin PLCC and PQFP and specified for the  $-40$  to  $+85^{\circ}\text{C}$  range. Prices start at \$35 in 100s.

*The AD7716 was designed at ADI's facility in Newbury, England, by a team led by Bob Brewer and Paul Shepherd.*

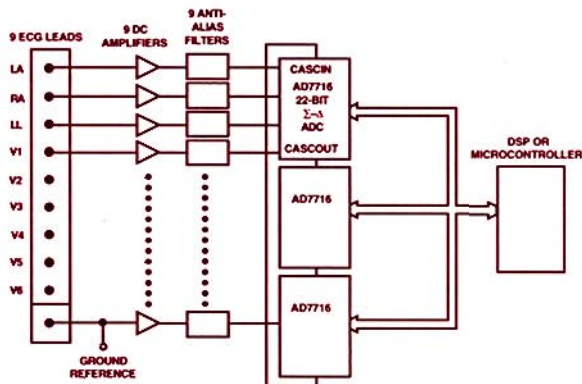


Figure 3. 12-lead ECG system using 4-channel sigma-delta converters.

\*For technical data use the reply card. Circle 2



# GSM Chip Set Implements All Baseband Functions

## AD20msp410 includes DSP, microcontroller, and codecs

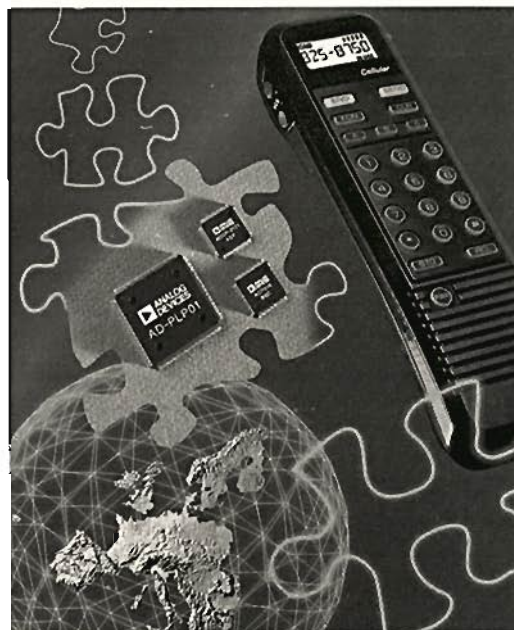
by Rupert Baines

The AD20msp410\* chipset integrates all the circuitry (3 chips) and software required to implement the baseband portion of a Phase 2 GSM [Global System for Mobile (communications)] handset. Developed with the assistance of The Technology Partnership (Cambridge, England), it needs only a radio subsystem—plus basic memory, keyboard, and display—to make a complete GSM handset. [A reference design for the RF stage is available, and Analog Devices parts will be available early next year.]

Here are the component parts: (see Figure 1):

- **ADSP-TTP01** digital ASIC (the physical layer processor, or PLP) performs all channel-coding functions and includes an embedded H8 16-bit microcontroller, which runs the complete protocol stack and application software,
- **ADSP-2171 DSP**, functions as an algorithm signal processor (ASP), for speech coding and soft-decision equalizing.
- **AD7015** dedicated mixed-signal device (baseband converter, or BBC) includes codecs and implements all mixed-signal radio, audio, and auxiliary functions of the terminal.
- **Software:** Layer 1 is supplied in firmware, while layers 2 and 3 are available as options.

What is GSM? The conventional cellular phone system is an analog system; the user's voice is carried as an analog waveform, while the control signals between the phone handset and base station are digital. In many parts of the world, newer digital standards are being implemented, where the voice is immediately digitized at the handset. In the U.S., two rival systems are being evaluated, IS54 (TDMA) and IS95 (CDMA), but the GSM digital standard (originally developed in Europe) is the most mature, with almost two million subscribers in forty countries.

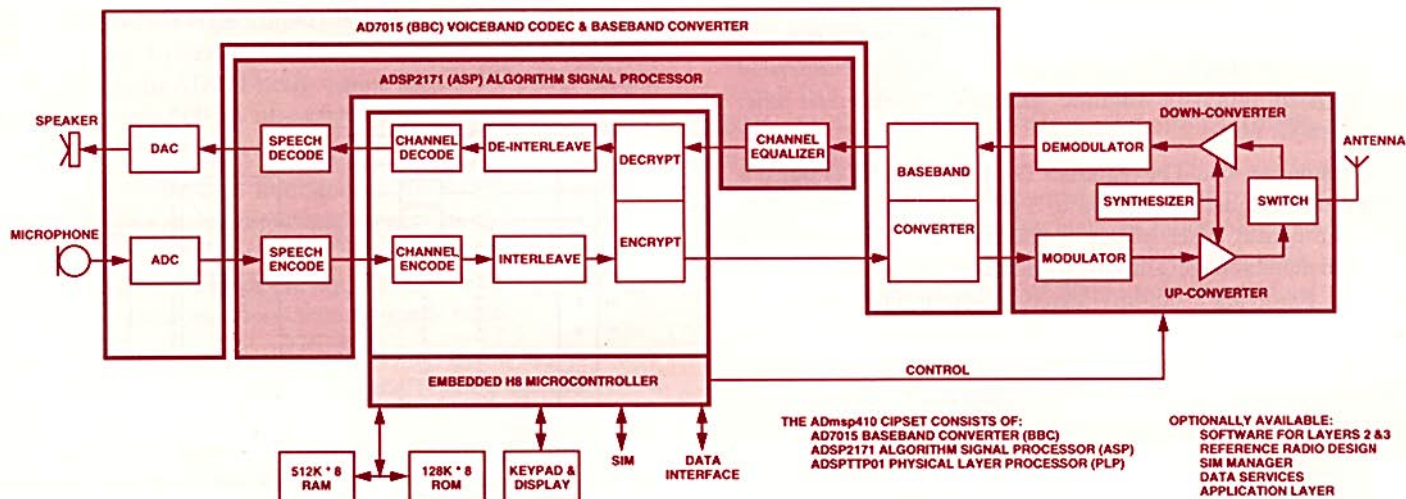


In a digital phone (see *Analog Dialogue* 26-1, page 5), voice-bit processing greatly reduces the required number of bits (hence bandwidth); error-correcting bits are added for robustness.

The present GSM system is being enhanced by *Phase 2*, with several compatible upgrades—including voice mail and direct digital services—and *half-rate* (one-half the bit rate for reduced-bandwidth requirements). Variations on GSM include DCS-1800 and PCS-1900, which use the same protocol at high carrier frequencies of 1.8 and 1.9 GHz for use with the smaller cells of personal communications networks (PCN). The AD20msp410 chip set supports all of these, merely by changing the final RF carrier.

Handsets require small size and low power; all three sub-micron CMOS parts operate from 3 or 5 V, with several power-saving modes, providing >2 hours of talk time and >40 hours standby.

They are packaged in compact TQFPs (176, 128, and 80 pins, respectively, for the PLP, ASP, and BBC) and occupy less than 12 cm<sup>2</sup> of board space. Just 1.4 mm high, they are small enough to fit into a Type 2 PCMCIA card. All parts of the system, including an evaluation board, are available for sampling. The chipsets and software are available separately or bundled. Chipset prices are <\$50 in OEM quantities. ▣



\*Use the reply card for technical data. Circle 3

Figure 1. System block diagram



# Two New LVDT Interface ICs Offer Choice of Analog or Digital Output

## AD698 universal LVDT signal conditioner and AD2S93 LVDT-to-digital converter

By Dan Williams

Despite the proliferation of linear displacement sensors using new technologies such as microwaves, lasers and magnetostriction, the linear variable differential transformer (LVDT) remains popular due to its inherent simplicity and ability to work in unimaginably nasty environments.

LVDTs find use in a wide range of applications, from positioning industrial robots to gauging the thickness of rolled steel to indicating aileron position in aircraft. Because of this diversity, there are thousands of different LVDT types in a variety of sizes, measurement ranges, and excitation frequencies. Considering the variety of LVDTs and controllers available, the question is, "How do I make my chosen LVDT talk with my chosen controller?"

The traditional answer has been costly, time-consuming home-grown solutions determined, to a large extent, by the type of analog or digital controller used. These solutions can now be replaced by two new ICs with a better answer. The AD698 signal conditioner and the AD2S93 LVDT-to-digital converter can interface a standard LVDT to any controller, analog or digital.

### HOW LVDTs WORK

Basically a transformer with a movable core (Figure 1), a typical LVDT consists of a fixed tube with a primary winding in the middle aligned with secondary windings at either end. In the center of the tube, attached to the source of motion, is a core of ferrite material, which is free to move along the tube's long axis.

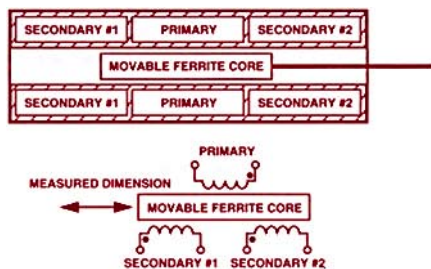


Figure 1. Physical and electrical construction of an LVDT.

LVDTs transformer-couple an ac reference signal from primary to the secondaries, producing a pair of ac-waveforms whose voltage ratio is proportional to the longitudinal displacement of the ferrite core. When it is centered on the primary, the signals induced in the secondary windings are equal. In most applications, the secondary windings are connected in series opposition so as to produce a null when the core is in the center position. As the core moves toward a secondary winding, its voltage increases, while

the voltage in its counterpart decreases. Phase of the output, relative to the reference signal, indicates which side of the null position the core is on.

**AD698 universal LVDT signal conditioner:** The AD698\* provides excitation (a low-distortion sine wave from 20 Hz to 20 kHz) and conditioning necessary to decode the output of LVDTs connected in half-bridge and series-opposed configurations. It produces a dc-output voltage, which represents linear position. Two synchronous demodulation channels detect the primary and secondary amplitudes, then the secondary amplitude (with correct sign) is divided by the primary to produce a normalized ratiometric output. This approach eliminates scale-factor errors due to primary amplitude drift with time, temperature, and loading—and improves interchangeability.

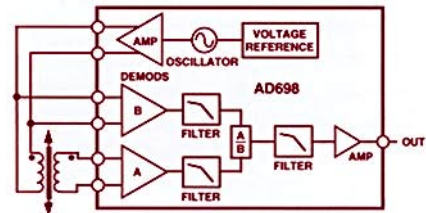


Figure 2. Block diagram of AD698 LVDT signal conditioner.

The AD698 is available in 28-pin PLCC and cerdip specified over the extended industrial (-40 to +85°C) and military (-55 to +125°C) temperature ranges. Pricing begins at \$8.19 (1000s).

**AD2S93 LVDT-to-digital converter:** The AD2S93\* converts LVDT outputs directly to digital, using a type II servo-loop. It continuously tracks the LVDT input without external wait or convert commands. Supplied with  $\pm 5$  V and a 360 Hz-to-10-kHz, 2-V rms reference signal, the AD2S93 accepts nominal 1-V rms signal inputs. An ac ratio bridge with phase-sensitive detector, integrator, voltage controlled oscillator (VCO), and up-down counter form a closed loop system (Figure 3), which continuously seeks to null the ACERROR output. When in lock, the word state of the up/down counter equals the LVDT position. When selected, the AD2S93 latches and outputs a 16-bit serial word, comprising 12-bits of displacement plus a sign bit (for the central two quadrants from the null position), over- and under-range bits, and a loss-of-signal bit. Remote diagnostics can be implemented by a controller reading the AD2S93's output.

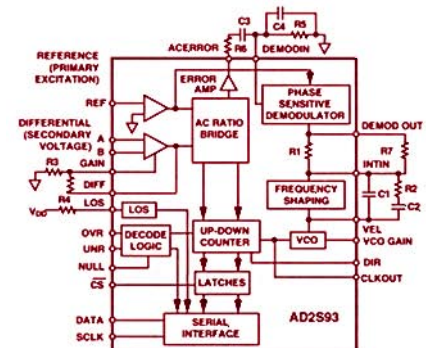


Figure 3. Block diagram of AD2S93.

Available in a 28-pin PLCC, the AD2S93 is specified to operate from -40 to +85°C. Prices begin at \$13.72 (1000s).

*The AD698 was designed by Larry DeVito, in Wilmington MA, and the AD2S93 was designed by Peter Johnson and Terry Searle in the UK.*

\*For technical data on these devices, use the reply card. Circle 4







# Fast Op Amp: High Performance, Low Power, Low Cost

**AD8001: 800-MHz BW @ G=+1,  
55 mW max ( $I_Q=5.5$  mA @  $\pm 5$  V)  
Diff. gain & phase: 0.01%, 0.025°**

The AD8001\* is a low-power, high-speed op amp designed to operate on  $\pm 5$ -volt supplies. It requires only 55 mW maximum quiescent power, yet it has a bandwidth of 800 MHz at unity gain and can furnish output currents of up to 70 mA. It is fabricated on the Analog Devices XFCB (eXtra-Fast Complementary Bipolar) process, which, with its low junction capacitance, allows the AD8001 to run at higher speeds while using less power than conventional CB processes. In addition, the process allows for smaller-geometry transistors, hence more dice per wafer, and therefore small size and low cost. It is packaged in 8-pin plastic DIP and SOIC packages for  $-40$  to  $+85^\circ\text{C}$  operation. Price is only \$2.75 in 1000s.

As the first of a new generation of amplifiers, the AD8001 avoids compromises and tradeoffs (performance vs. power dissipation vs. price) that were necessary in earlier generations.

A current-feedback device, it can be used as an amplifier or buffer and to drive cables for any high-speed signal, including video and RF. Because of its low power consumption, it can be used in power-sensitive high-speed applications, such as portable communications, video equipment and multi-channel systems requiring many high-performance amplifiers. It is also ideal as a high-speed buffer between precision analog circuitry and A/D converters, because of its fast settling and low distortion.

**Wide bandwidth:** Figure 1 is a plot of the device's small-signal frequency response at a gain of +2, while driving a 100- $\Omega$  load. At gain of +1, with  $R_{FB} = 1$  k $\Omega$ , the  $-3$ -dB bandwidth is 650 MHz minimum, 880 typical, with  $<1$ -dB peaking (DIP). It will maintain 0.1-dB flatness to 100 MHz minimum at a gain of +2 (SOIC). These characteristics are useful in video and RF—as well as general high-speed—applications.

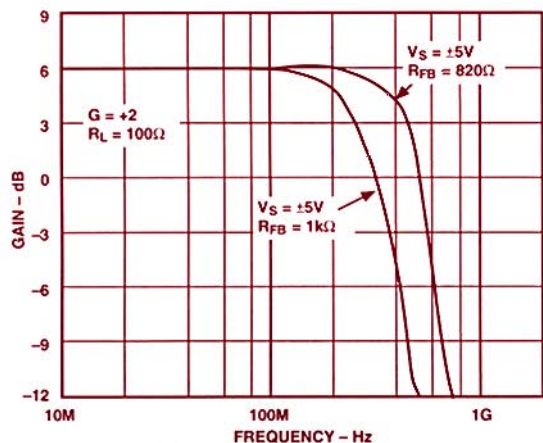


Figure 1. Frequency response of the AD8001 at gain of +2 V/V with 100-ohm load.

**Excellent dynamic specs and low distortion:** Figure 2 shows the device's fast, clean, non-ringing response for a 2-V square-wave output at gain of +2; it slews typically at 1000 V/ $\mu\text{s}$  (800 minimum). At gain of  $-1$ , it settles to within 0.1% in 10 ns, with a typical slew rate of 1200 V/ $\mu\text{s}$ . The AD8001 has the lowest distortion of any amplifier running on 50 mW of power:  $-65$  dBc at 5 MHz. In addition, its SFDR is  $-66$  dB at 5 MHz, and 3rd-order intermodulation-distortion intercept (see page 5) is 33 dBm at 10 MHz. The AD8001 is an excellent buffer for A/D converters.

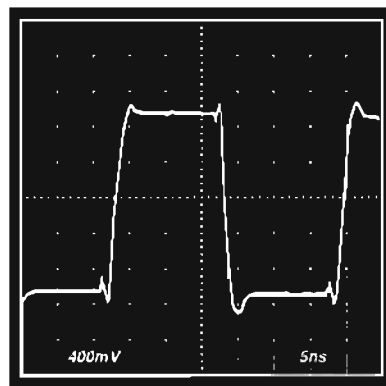


Figure 2. Transient response of the AD8001 for a 2-V output step at a gain of +2.

**Video and output-current specs:** Even though the AD8001 runs on only 5.5 mA of supply current, it provides excellent differential gain (0.01%) and phase (0.025°) characteristics, with 0.1-dB gain flatness to 100 MHz while driving a 150- $\Omega$  load. Its 70-mA (50 mA min) output current provides sufficient drive for four 75- $\Omega$  back-terminated loads (37.5  $\Omega$ ), while maintaining differential gain and phase of 0.05% and 0.25°.

Figure 3 shows the AD8001 in a line-driver application with a pair of back-terminated 75- $\Omega$  loads (0.01%, 0.07°). Isolation between loads is 40 dB at 5 MHz in this application.

**Ease of use:** For a device having such wide bandwidth, the AD8001 is remarkably easy to use. It is stable and free from parasitics. Evaluation boards are available, along with a comprehensive 16-page data sheet.

*The AD8001 was designed by Scott Wurcer at our Wilmington MA facility.*

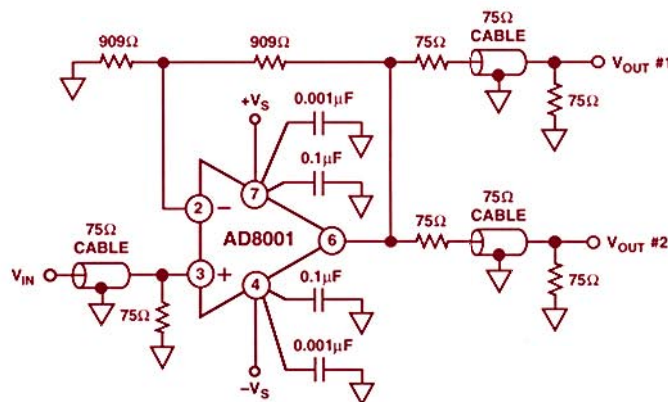


Figure 3. Video line-driver application—driving two back-terminated loads.

\*Use the reply card for technical data. Circle 8



# Microphone Preamplifiers for Audio

## A brief guide for users

by Walt Jung

### INTRODUCTION

Audio signal preamplifiers (preamps) deal with low-level signals in practical audio circuits using modern IC devices. In general, preamps are amplifying stages with input signal levels of 10 mV or less. This article discusses two basic types of audio preamps suitable for use with microphones.

When working signals drop to a level of 1 mV, the input noise generated by the first amplifying stage in a system becomes a critically important consideration when designing for best dynamic range and signal-to-noise ratio. For example, if in a given band, the internally generated noise voltage of an input stage is 1  $\mu$ V and the input signal voltage is 1 mV or less, the very best signal-to-noise ratio one can expect is only 60 dB.

In a preamp application, the impedance of a source is usually fixed, and the signal dynamic range has an upper limit. Thus, for best signal-to-noise ratio with a given source, the input noise generated by the first amplifying stage must be minimized. This factor has definite implications for a preamp designer, since a "low-noise" circuit for a low-impedance source can be quite different from a low-noise preamp designed to operate from a high impedance. The rules of semiconductor physics drive these decisions,[1] but in broad terms one can expect to employ bipolar junction-transistor (BJT) input stages for lowest additional noise with low-impedance sources (<1 k $\Omega$ ), and junction FET (JFET) input stages with high impedance sources (>10 k $\Omega$ ). For intermediate source impedances, either type of input stage might be used, depending on the particular amplifier characteristics and source impedance.

Successfully minimizing the input noise of an amplifier requires a full understanding of all the various factors that contribute to total noise. These include the amplifier itself, the external circuit, and in truth, the total circuit environment. All must be considered, to minimize noise and maximize both dynamic range and general signal fidelity.

Another design consideration is that, in addition to achieving a basic gain or signal scaling function, frequency response may also need alteration in a predictable manner. The microphone preamps discussed here are examples of wideband, flat-response, low-noise amplifiers. In contrast to this, preamps for phonograph and tape circuits not only scale the signal; they also impart a specific frequency-response characteristic.[2]

### MICROPHONE PREAMPLIFIER TYPES

The microphone (mic) preamp is a basic circuit requirement among low-level audio amplifiers. Mic preamps can assume a variety of forms, considering the variety of microphone impedance and other characteristics, wide range of possible signal levels, and methods of interfacing. These factors influence the optimum circuit choice for a specific application. This article addresses preamps for *low-impedance balanced microphones*, a type of source that almost invariably requires devices employing bipolar input transistors to achieve best noise performance.

The circuit examples shown can be used both with and without "phantom" power\*, and with input stages that may or may not use transformers. An earlier article discussed a single- or dual supply mic preamp, suitable for single-ended high-impedance sources. [3] Also, while not a preamplifier circuit *per se*, an interface for electret mics has been described elsewhere.[2]

With the extremely wide variety of amplifiers available to a designer, op amp selection for many applications is usually pretty straightforward. An important element is optimizing the choice of amplifier for the specific application based on voltage and current noise parameters, bearing in mind that voltage and/or current noise effects can be dominant and that there is no such thing as the "universal" low-noise amplifier.

### Transformer-coupled low-impedance mic preamps

For any op amp, the best noise performance is attained when the characteristic noise resistance of the amplifier,  $R_n$ , is equal to the source resistance,  $R_s$ . This section discusses examples of microphone preamps that employ this principle and utilize an input transformer to more closely match impedances when  $R_n$  and  $R_s$  are not equal to one another.

A basic transformer-coupled circuit is shown in Figure 1. In order to select an optimum turns ratio to match a given source resistance ( $R_s$ ), the characteristic  $R_n(U1)$  of the op amp U1 must first be calculated from data for  $e_n$  and  $i_n$ , as follows:

$$R_n(U1) = \frac{e_n}{i_n} \quad (1)$$

where  $e_n$  and  $i_n$  are audio-band voltage and current noise spectral densities, in  $V/\sqrt{Hz}$  and  $A/\sqrt{Hz}$ , for the op amp being considered for U1. Best results are obtained in practice with a low-voltage-noise amplifier that meets the criterion.

The values for  $R_s$  and  $R_n$  can be used to calculate a turns ratio for T1:

$$\frac{N_s}{N_p} = \sqrt{\frac{R_n}{R_s}} \quad (2)$$

where  $N_s/N_p$  is the transformer secondary/primary turns ratio. For op amps such as the OP176 and OP275, the values of  $e_n$  and  $i_n$

\*An external supply powering the signal source—usually a capacitance-principle microphone and its associated circuitry; this requires the preamp designer to deal with up to 48 volts of common mode.

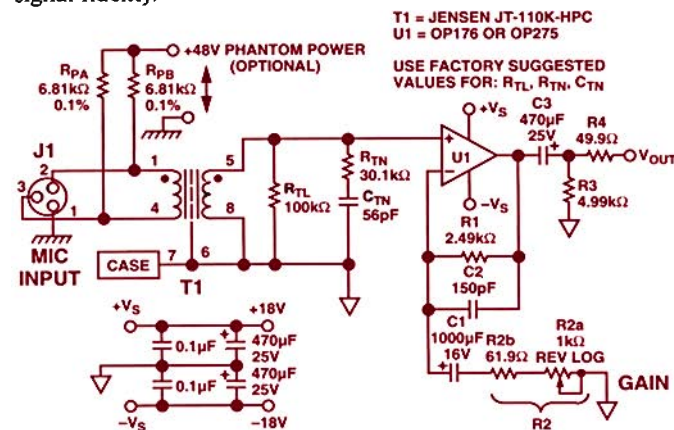


Figure 1. Transformer-input mic preamp with 28-50-dB gain.

are 6 nV/√Hz and 0.5 pA/√Hz, respectively; thus,

$$R_{n(U1)} = \frac{6 \times 10^{-9} V}{0.5 \times 10^{-12} A} = 12 \text{ k}\Omega$$

Since both  $e_n$  and  $i_n$  vary with frequency,  $R_n$  will also vary with frequency. Therefore, a value calculated for  $R_n$  from the data sheet (such as above) is most accurate at the specified frequency. If the choice of amplifier is to be optimized for a specific frequency, then the  $e_n$  and  $i_n$  values should be for that frequency. However audio amplifiers are wide-band circuits, and transformers are non-ideal devices; some compromise may be necessary here. When available, a minimum noise figure plot for the amplifier allows the optimum source resistance for least noise to be determined graphically.

For this case, equation (2) can be used to calculate an optimum transformer turns ratio for optimum  $R_{n(U1)}$ , working from a given  $R_s$ . For example, if  $R_s = 150 \Omega$ , an optimum turns ratio for an OP176 (or an amplifier with similar noise specs), with an  $R_n$  of 12 kΩ, will be:

$$\frac{N_s}{N_p} = \sqrt{\frac{12 \times 10^3 \Omega}{1.5 \times 10^2 \Omega}} \approx 8.9$$

This ratio is close to a round-number 10:1 ratio; it is suitable for other op amps with roughly similar  $e_n/i_n$  (and thus  $R_n$ ), for example OP27 or OP37 types, the OP275, OP270/470 types, as well as industry-standard 5534 or 5532 types. Since low-level audio transformers are somewhat specialized and not available over broad impedance ranges, a unit with a rated secondary impedance in a range of 5 kΩ to 15 kΩ will be about right (since the amplifier's minimum noise impedance of itself has a reasonably broad range of variation). Examples of units suitable for this purpose are Jensen Transformer types JT-13K7-A, JT-110K-HPC, and the JT-115K-E. [4] In any case, T1 must have adequate magnetic and electrical shielding, and be otherwise suitable for operation in low-level environments.

The use of a matching transformer allows the circuit to achieve an equivalent input noise (referred to the transformer input) only a few decibels above the theoretical limit, or very close to the thermal noise of the source resistance. For example, the thermal noise of a 150-Ω resistor in a 20-kHz noise bandwidth at room temperature is 219 nV. For an actual circuit, the total input-referred noise is higher because of noise contributed by the transformer and the op amp.

An additional advantage of the transformer is that it provides effective voltage gain, due to the step-up turns ratio. For a given overall numeric gain,  $G_{total}$ , this reduces the gain required from the op amp U1,  $G_{(U1)}$ , to:

$$G_{(U1)} = \frac{G_{total}}{N_s/N_p} \quad (3)$$

So, in the composite circuit of Figure 1, the total gain,  $G_{total}$  is the product of the transformer stepup,  $N_s/N_p$ , and  $(R_1 + R_2)/R_1$ , or  $G_{(U1)}$ . This allows more amplifier-circuit loop gain, with greater bandwidth and accuracy, lower distortion, etc.

The mic preamp stage in this transformer input example uses the JT-110K-HPC transformer for T1, with a stepup turns ratio of about 8 (equivalent to an impedance ratio,  $N_s^2$ , of 10 kΩ/150 Ω). The op amp section has a variable gain of about 3.3 to 41 V/V (i.e., 10.4 to 32.3 dB); cascaded with the 17.8-dB transformer

gain, it yields a composite gain of 28 to 50 dB (26 to 328 V/V). Transient response of the composite amplifier (transformer plus U1) is excellent when connected as shown. It is important that the manufacturer's recommended secondary loading network ( $R_{TL}$ ,  $R_{TN}$  and  $C_{TN}$  in the figure) be used, for flattest response from the rated source impedance.

The amplifier used as U1 is either a single OP176, or alternately an OP275 section. U1 operates here on supplies of ±18 V (up to ±22 V maximum), and can drive 600 Ω. The power supplies used should be well-regulated, with decoupling close to U1, particularly when low impedance loads are driven.

For best results, passive components in this circuit—and those that follow—should be high-quality, e.g., 1% metal-film resistors, a reverse log taper film pot for R2A, and low ESR capacitors for C1 and C3. The circuit is easily adapted for microphone phantom powering, by adding the matched  $R_{PA}$  and  $R_{PB}$  6.81-kΩ resistors, with a 48-V dc source as shown. [5,6] Close matching (±0.1%) of the two dc feed resistors is recommended by the transformer manufacturer whenever phantom power is used, to both optimize common-mode rejection (CMR) and minimize the transformer's dc primary current. [7]

In this configuration, phantom powering has little or no effect on the amplifier circuitry, since the transformer decouples common mode (CM) dc variations at the primary. CMR for an input transformer, such as the JT-110K-HPC, is typically 85 dB or more at 1 kHz—and substantially greater at lower frequencies. Lower impedance-ratio types, such as the JT-16A (below), have higher 1-kHz CMR, typically, 100 dB.

The -3-dB bandwidth of this circuit, dominated by the JT-110K-HPC transformer and its termination network, is about 100 kHz, assuming a 150-Ω source impedance. For higher or lower source impedances, the bandwidth will decrease or increase in proportion, a factor that should be taken into account when applying this circuit. Some provision should be made to control the working source impedance with a build-out pad ahead of the transformer, when the circuit is to be used with source impedances lower than 150 Ω. [7] For example, capacitor microphone capsules using emitter followers have output impedance that looks to the preamp like an approximately 15-Ω source.

The family of curves in Figure 2 shows typical THD+N performance of this mic preamp (% of signal), using either the OP275 or the OP176. The test is run at 35-dB gain, with frequency swept at successively increasing input levels, for outputs of 0.5, 1, 2, and 5 V rms into 600 Ω. This technique, using successive sweeps, is useful for testing sensitivity to slewing-related distortions. Sweeps with different output loads are useful for testing sensitivity to load-related non-linearity. Amplitude and frequency dynamic tests can be combined for characterizing the effects of both device and circuit. [8]

For the data presented in Figure 2, there exist three regions of interest: a low-frequency region below 100 Hz, where distortion increases rapidly with decreasing frequency, largely due to the transformer; a low-distortion mid-band region from 100 Hz to 3 kHz, principally dominated by noise; and the region above 3 kHz, where the distortion increases with frequency and level. Over most of the frequency range (40 Hz to 10 kHz), THD+N is ≤0.01%.

Although this transformer-input preamp has been discussed in terms of a low impedance source (microphone), the transformer-



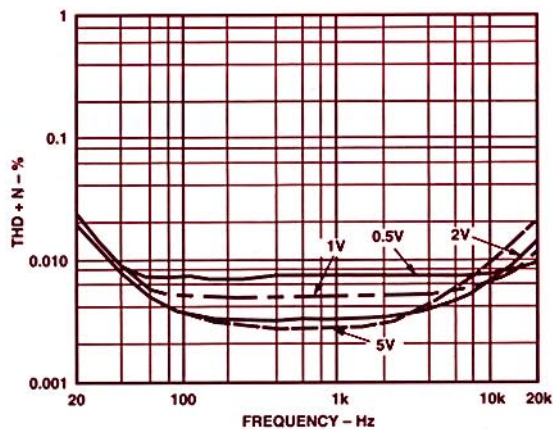


Figure 2. Transformer-input mic preamp THD+N (%) vs. frequency (Hz);  $V_{out} = 0.5, 1, 2,$  and  $5\text{ V rms}$ , gain = 35 dB,  $R_L = 600\ \Omega$ ,  $U1 = OP275$ .

impedance-matching technique can apply to transducers with higher impedance. It is only necessary to know the characteristic noise resistance of the op amp. If this data is not given in terms of  $\epsilon_n$  and  $i_n$ , it can be determined from curves of noise figure versus source resistance. Since the noise figure is at a minimum when  $R_n = R_s$ , the source resistance for minimum noise figure will be very close to  $R_n$ . This value can then be used in selecting the transformer turns ratio to match the transducer to  $R_n$ .

### A very low noise transformer-coupled mic preamp

A high-performance transformer-coupled low noise mic preamp is shown in Figure 3, using an op amp with less voltage noise, the AD797. With the lower-noise op amp, a transformer with an appropriately lower ratio can be used—the JT-16A, with a nominal step-up ratio of about 2:1; it is optimized towards use with lower noise-resistance amplifiers. The AD797 used here has  $R_n$  of  $(0.9\text{ nV}/\sqrt{\text{Hz}})/(2\text{ pA}/\sqrt{\text{Hz}})$  or  $450\ \Omega$  at 1 kHz. The rest of the circuit has a topology somewhat similar to that of Figure 1, but there are differences in the details to arrive at premium levels of performance. The AD797 is used for both lowest noise and lowest distortion; for best results, the designer should employ its unique distortion-cancellation capacitor, C2. [9] The circuit can drive single ended outputs, or it can be coupled to balanced lines with the use of the optional transformer, T2, as shown.

This preamp has a switch-selectable variable-gain feature, using switch S1 to alter  $R_2$  of the feedback network so as to vary  $U1$ 's

gain (and thus the overall gain) according to the table of Figure 4. The range chosen is 20-50 dB, suitable for a wide range of uses, and gain is selectable in 5-dB increments. The low resistance values in the network at the highest gains produce lowest resistor noise at signal levels where low noise is most needed.

Total Gain, dB	U1 Gain, dB	R2 (Total), $\Omega$	"R2N", $\Omega$
50	44.4	15.15	15.0
45	39.4	27.07	11.8
40	34.4	48.56	21.5
35	29.4	87.68	39.2
30	24.4	160.3	73.2
25	19.4	300	140
20	14.4	588.5	287

T1 Provides a Fixed 5.6dB Gain.  
R2N is individual R2A, R2B, etc.  
Closest Standard Values are Shown.

Figure 4.  $R_2$  gain table for circuit of Figure 3, 20-50-dB gains.

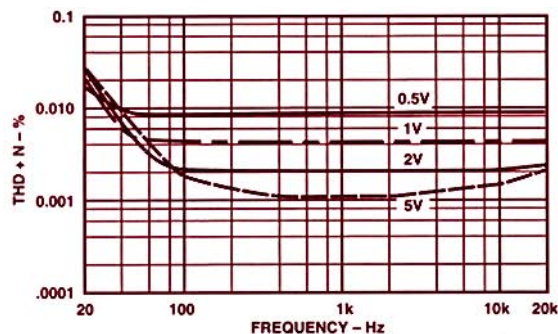


Figure 5. Low-noise transformer-input mic preamp, THD+N (%) vs. frequency (Hz);  $V_{out} = 0.5, 1, 2,$  and  $5\text{ V rms}$ , gain = 35 dB,  $R_L = 600\ \Omega$ .

A servo loop is used to minimize output dc offset from  $U1$ ; low offset is necessary for direct and/or transformer coupling (T2). An integrator ( $U2A$ ) monitors the output of  $U1$  and feeds back a correction voltage to  $U1$ 's negative input; in the steady state, the average output of  $U1$  is equal to the low offset of  $U2A$  (i.e.,  $V_{os} + I_b R_o$ ). Because of the method by which the servo's dc feedback is added at  $U1$ 's summing point, this loop's time constant doesn't change when the gain is changed by switching resistors  $R2x$ . Consequently, the preamp's low-frequency rolloff is independent of gain.

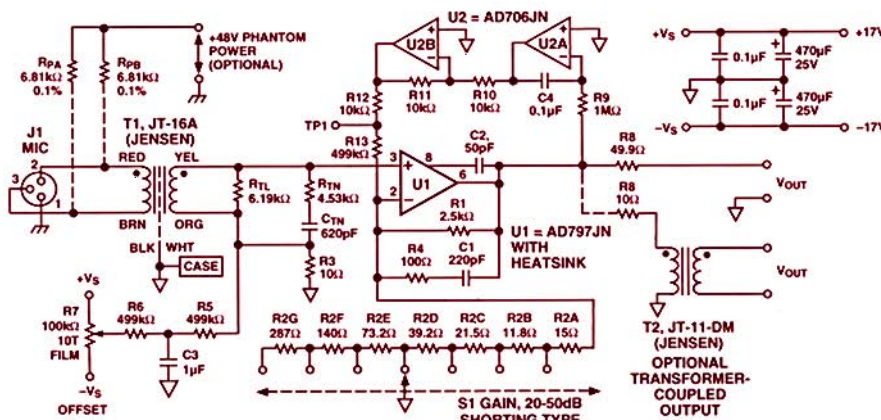


Figure 3. Low-noise transformer-input microphone preamp.

Because the AD797 combines high dc precision with low-distortion audio characteristics, this circuit can be dc-coupled quite effectively. However, if transformer T1's common lead (ORG) were to be grounded directly, U1's inherent offset would appear at the input, and the current change through the R2x string when the gain is switched could cause audible clicks. The AD797's initial offset (80  $\mu\text{V}$  max), can be trimmed using R7 to bias the + input. To perform the initial adjustment of R7, the output offset is manually trimmed with the servo temporarily defeated by grounding test point TP1, using a mid-range gain of 35 dB. The output dc is easily trimmed to within 1 mV (<34  $\mu\text{V}$  at the -input). The resulting output offset shift with gain change is only a few millivolts and is of little concern, since the servo circuit typically holds longer-term dc offset to 100  $\mu\text{V}$  or less, with very little gain interaction.

(THD+N)/signal [THD+N = total harmonic distortion + noise] performance is shown in Figure 5. The test is run at 35-dB gain, with frequency swept at successively increasing input levels, for outputs of 0.5, 1, 2, and 5 V rms into 600  $\Omega$ , using an analyzer with 80-kHz bandwidth. From these data it can be ascertained that essentially the only distortion in the circuit is due to the transformer: it is quite low and is significant only at the very lowest frequencies. Above 100 Hz, THD+N is mainly determined by noise (and thus inversely amplitude-related), continuing through to the highest frequencies, except for slightly increasing distortion at 5-V rms.

The -3-dB bandwidth of this circuit (Figure 6) is just under 150 kHz; the response is shown for the two operating gain extremes of 20 and 50 dB. While bandwidth is essentially dominated by the JT-16A transformer and termination, it is reduced slightly at the highest gain of 50 dB (lower curve). Like the circuit of Figure 1, this circuit also presumes a 150- $\Omega$  source impedance; it requires similar caveats in application. Reference[7] includes information on both build-out and fixed-loss input pads, and other practical interfacing considerations for transformers.

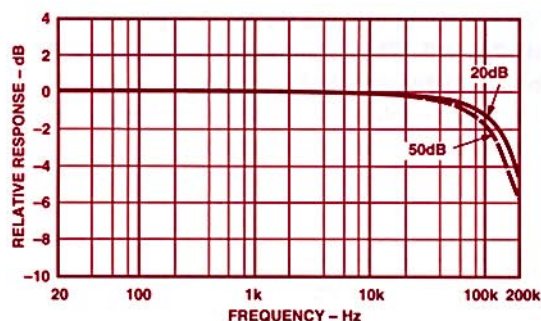


Figure 6. Low-noise transformer-input mic preamp, relative gain (dB) vs. frequency (Hz);  $V_{\text{out}} = 1$  V rms, gain = 20 and 50 dB,  $R_L = 600 \Omega$ .

The basic output as shown is single-ended, with  $V_{\text{OUT}}$  taken from R8, but a transformer can be optionally added to drive balanced lines and provide isolation. If used, T2 is a JT-11-DM (or similar) nickel-core type for lowest distortion; it is coupled to U1 as shown, via the alternate connection and value for R8.

If very high levels of output drive are necessary or long lines are to be driven, a dedicated high-current output driver should be used with U1, as described in "Line Drivers" section of [2]. This can

be most easily implemented by making U1 a composite amplifier employing an AD797 input section plus a unity-gain follower output stage, using the AD811.

Noise of the preamp of Figure 3, while low, also depends on the gain setting. It is lowest at the highest gains, and conversely higher when gain is low. The noise of the preamp was analyzed using an Audio Precision System One operating in a bandpass sweep mode. This test sweeps a device under test over a specified range, measuring the rms noise output with the input terminated, in this case with 150  $\Omega$ . The 1/3-octave bandpass filter used in this analyzer mode has a noise bandwidth of  $0.2316 \times F$ , where  $F$  is the filter center frequency.

To convert the measured noise voltages to an equivalent input noise voltage density,  $e_n$ , the relationship below is used:

$$e_n = \frac{\text{measured noise}}{(G) \times \sqrt{0.2316 F}} \quad (4)$$

where  $G$  is the amplifier gain (V/V),  $F$  is the particular frequency neighborhood of interest, and "measured noise" is the actual rms noise measured at that gain/frequency. Note that gain settings of 20, 35 and 50 dB correspond to gain ratios of 10, 56, and 316 V/V.

Referring to the noise plot of Figure 7, for a gain of 50 dB and at a frequency of 1 kHz, the measured noise is 10  $\mu\text{V}$ , therefore  $e_{n(50)}$  calculates as:

$$e_n = \frac{10 \times 10^{-6} \text{ V}}{3.16 \times 10^2 \times \sqrt{231.6 \text{ Hz}}} = 2.07 \text{ nV}/\sqrt{\text{Hz}}$$

As noted, equivalent input noise worsens at low gain in reality, as also does the uncertainty in measurement. Similar measurement and calculations for gains of 35 and 20 dB yield  $e_{n(35)}$  of 2.3, and  $e_{n(20)}$  of 3.6  $\text{nV}/\sqrt{\text{Hz}}$  (the corresponding plots are not shown). As a point of reference, a 150- $\Omega$  resistor has an  $e_n$  of 1.55  $\text{nV}/\sqrt{\text{Hz}}$ .

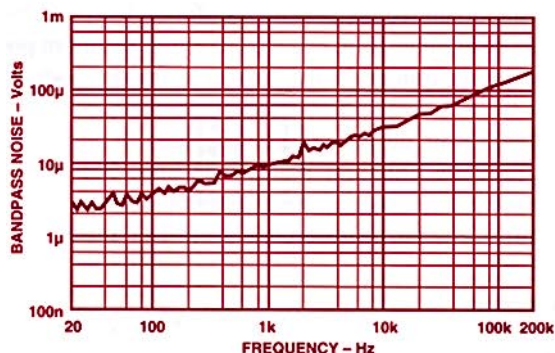


Figure 7. Low-noise transformer-input mic preamp, bandpass filtered output noise (V) vs. frequency (Hz); gain = 50 dB,  $R_S = 150 \Omega$ .

### Transformerless-input low-impedance mic preamp

Another way to amplify low-level balanced mic signals is to use a transformerless differential input stage, with an instrumentation amplifier (in-amp) as the preamp. The in-amp (in IC or other form) is configured for gain with just one resistor. It provides transformerless gain with good rejection of audio-band CM noise, such as hum, and—using a suitable low-noise amplifier—has low operating noise with commonly used low-impedance mics.



Figure 8 is an example of a low-noise transformerless mic preamp, using the SSM2017P preamp IC as U1, and a pair of OP176 op amps for U2 and U3, as a servoed buffer. The preamp, which has an optional phantom power feature, has a gain adjustable from 6 to 66 dB.[10]

Features rendering the SSM2017 suitable for use in transformerless mic preamps include low input noise of less than  $1 \text{ nV}\sqrt{\text{Hz}}$ , plus high CM rejection and low distortion. Gain of this 8-pin IC is set via one external resistor,  $R_G$ , and is adjustable over a range of 1 to 1000 V/V (0 to 60 dB). Differential inputs at pins 2-3 allow balanced-mode input signals, with a single-ended output signal developed between the output (6) and reference (5) pins.

The SSM2017 is used advantageously in a gain-programmable input stage, which then drives a fixed-gain-of-2 OP176 high-current output buffer, U2, with an associated dc servo, U3. The buffer, U2, provides low distortion drive into 600-ohm loads, and the servo, U3, maintains low output dc offset ( $\leq 1.5 \text{ mV}$ ).

In the U1 stage, gain is set by resistance,  $R_G$ . With the fixed gain of 2 in the U2 stage, the preamp's overall gain,  $G$ , is:

$$G = 2 \times \left[ \frac{10,000 \Omega}{R_G} + 1 \text{ V/V} \right] \quad (5)$$

$R_G$  can be either a reverse log-taper pot, or a switch-controlled resistance, used to control the gain of the entire circuit. The  $R_G$  value for a given gain,  $G$ , is:

$$R_G \left[ \frac{20,000 \Omega}{G - 2} \right] \quad (6)$$

Figure 9 tabulates  $R_G$  values for various gains, using the closest standard 1% resistor values. Since  $R_G$  is located at a low-level point in the circuit, it should be physically close to U1. Do not use long leads to a remote gain control; instead, an extended mechanical coupling is preferable.

Another important requirement for transformerless preamps is that they must be immune from being damaged by phantom power. In phantom-powered microphone circuits, common-mode 48-V dc power is fed to a remote mic capsule; the balanced audio signal received back from the mic must be amplified cleanly with no side effects from the phantom power's dc bias. For steady-state conditions this is simple, but switching transients from the dc power can readily kill an unprotected amplifier input stage. So

Gain	Gain in dB	$R_G (\Omega)^*$
2	6	Open
4	12	10,000
10	20	2,490
20	26	1,100
31.6	30	681
40	32	523
100	40	205
200	46	100
316	50	63.4
400	56	49.9
1000	60	20
2000	66	10

\* $R_G$  is rounded to closest 1% value where noted.

Figure 9.  $R_G$  gain table for circuit of Figure 8, 6 to 66-dB gain.

transformerless mic preamps must be protected against power surges, but with minimal (if any) degradation of performance.

Normally, coupling capacitors  $C_{in1}$  and  $C_{in2}$  decouple the phantom power dc level, passing only the balanced audio signal to U1. But, when the phantom power is switched on/off or the mic cable is plugged in/out, potentially destructive transients of up to  $\pm 48 \text{ V}$  are coupled through  $C_{in1}$  and  $C_{in2}$ , and appear across  $R_{B1}$  and/or  $R_{B2}$ . If these transients are not safely dissipated, they can cause destruction of U1. This applies to virtually any amplifier input stage, not just the SSM2017, since energy stored in the coupling capacitors can develop peak discharge currents of several amperes.

In Figure 8, CM voltage limiting is used; each of the differential input lines is shunted by pairs of back-to-back low-voltage Zener diodes, Z1-Z2 and Z3-Z4—standard 400-mW,  $V_z = 5.1\text{-V}$  units from the 1N750 series. Peak-current limiting for transient discharge is provided by the protection resistors  $R_{p1}$  and  $R_{p2}$ .

This preamp can be operated with or without phantom power, so it is logical to optimize input connections so that those portions not absolutely essential for phantom power are not in the signal path when it is not in use, and the 48-V dc power itself should be switched off as well. When phantom power is used, the 48-V supply should be interlocked with the bipolar power supply of the amplifier to avoid inviting trouble; this will prevent applying phantom power with the amplifier circuitry powered down.

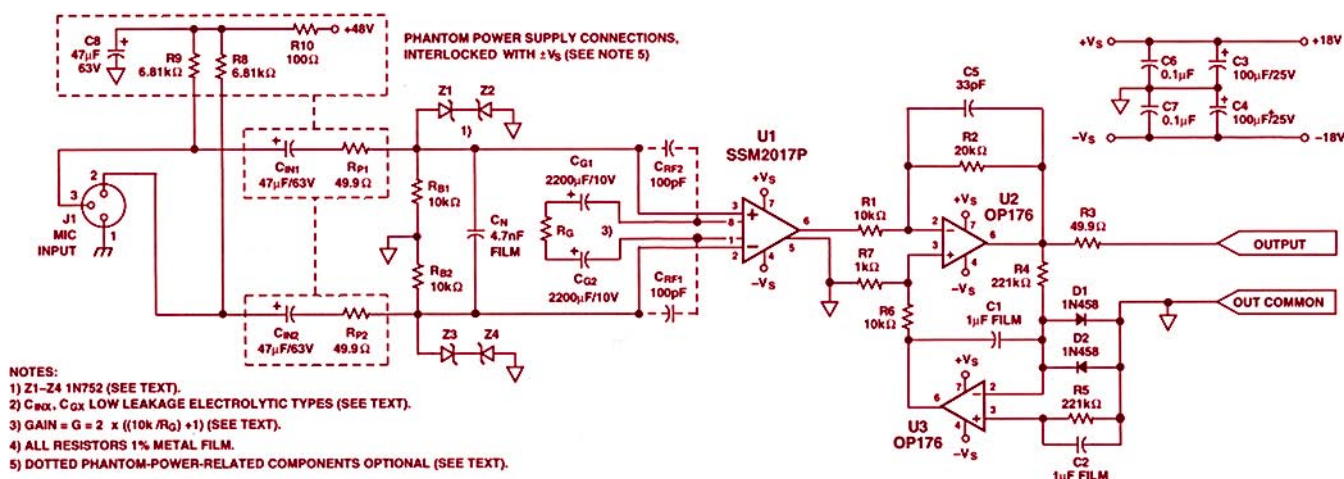


Figure 8. Low-noise transformerless-input microphone preamp.

Another source of potential problems with high-gain preamps is radio frequency interference (RFI). Here input capacitor,  $C_N$ , filters high frequencies above 135 kHz before they reach the preamp input. In addition, further filtering is provided in the second stage by  $R_2-C_5$ , at 241 kHz. Additional RFI filtering can take on several options, both in-circuit or on a system level (see *Box*). Within the circuit of Figure 8, separate low-resistance in-line RF chokes can be used in series with the two inputs, as can a single common-mode choke, chosen to reject the expected interference. RF bypassing of the SSM2017's input transistors can also be used, from pins 1-2 and 3-8 (shown optionally on the schematic as  $C_{RF1}$  and  $C_{RF2}$ ).

This amplifier's performance is quite good over programmed gain ranges of 6 to 66 dB (i.e., 2 to 2000 V/V). For a typical audio load of 600  $\Omega$ , the THD+N performance (Figure 10) at various gains and an output level of 10 V rms is consistent and well below 0.01%, for all but the highest gains, where it becomes principally limited by noise. Noise performance is quite good; at an operating gain of

1000, it is equivalent to 1 nV/Hz, referred to the preamp input. Maximum output is a function of the power supplies, and—as shown—can be as high as 10 V rms, with higher-voltage supplies. The series output resistor,  $R_3$ , does limit available swing somewhat in driving 600  $\Omega$ , but it should be retained for isolation and short-circuit protection. Supply voltages of  $\pm 18$  V or more are appropriate for highest output into 600  $\Omega$ , but lower supply voltage is appropriate for lower maximum output levels.

The SSM2017 device architecture is basically similar to that of family predecessors, SSM2015 and SSM2016, but the 8-pin package rules out access to the internal gain resistors. These devices, applied in circuits similar to Figure 10 with phantom powering, have individual virtues. For example, the SSM2016 can be applied with supplies of up to  $\pm 36$  V, and it has a high-current output stage ( $\pm 40$  mA minimum). This enables it to drive low-impedance audio loads to high levels without a buffer. ▶

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\*Book available for purchase from Analog Devices. Use book purchase card.

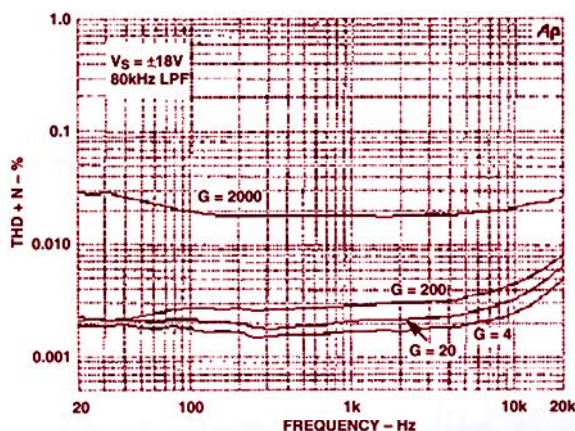


Figure 10. Low-noise transformerless-input mic preamp, THD+N (%) vs. frequency (Hz);  $V_{out} = 10$  V rms, gain = 12 to 66 dB,  $R_L = 600 \Omega$ .

## SYSTEM RF INTERFERENCE PREVENTION

As the main text notes, both circuit- and system-level perspectives may be required to prevent potential RFI problems with low level preamplifiers (such as mic preamps). System performance is impacted by both the topology chosen and the physical arrangement of components within a given circuit.

From a system point of view, the basic choice between transformer and transformerless preamp circuitry has a major impact on RFI sensitivity. This is so because a typical audio-grade transformer has high CMR and is a natural low-pass filter at RF. Thus, to at least a first order, a transformer-input mic preamp can be expected to have more RFI immunity than a transformerless design. The degree to which these expectations can be realized depends on both the relative frequency of the interfering signals and the transformer's physical construction.

On the other hand, a transformerless mic preamp would seem inherently susceptible to RFI problems, since it lacks an intrinsic low-pass filter (comparable to a transformer) preceding it. Yet, for the same application it must work from the same cable

lengths (read *antenna!*), as a transformer preamp type. Not only does the transformerless mic preamp lack up-front filtering, but the inherent design principles of low noise stages which make them attractive for mic preamps also tend to make them vulnerable to RFI.

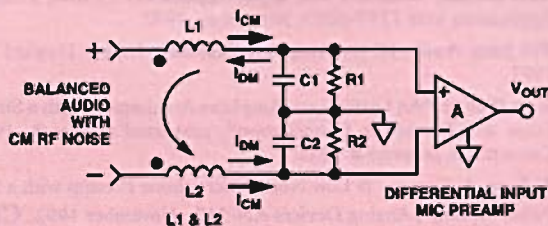
A low noise preamp input stage has high transconductance, and typically this means the use of bipolar transistors. While bipolars are indeed excellent for internally generated noise (transconductance and noise have an inverse relationship), their high transconductance at the same time also opens the door to greater RFI sensitivity. In fact, a comparison of bipolars versus FETs, in both op-amp and instrumentation-amplifier input stages, both in theory and experimentally, shows the bipolar stage more susceptible to RFI. [B1] The key application question then becomes what can one do in the circuitry external to a low noise mic preamp to obtain best RFI immunity.

While the relatively simple circuit measures of bandwidth limiting, such as those shown in Figure 8, can be helpful, they



may not be adequate when the preamp must work directly within a strong RF field—for example, in a radio-station studio adjacent to a transmitter. This problem can be most acute (and easiest to observe) when the RF is at a relatively low frequency, such as the standard AM broadcast band (0.5 to 1.5 MHz). This frequency span is difficult to filter with high attenuation, since it is only one decade (or less) above the approximately 100-kHz bandwidth typically used with mic preamps to avoid bandwidth limiting in multistage audio system applications. As a result, suppression of this interfering band by 40 dB or more is not at all a trivial matter when using conventional filtering. Interference at higher frequencies, for example, 10 MHz or more, does allow relatively simple R-C or L-C filters to be effective, typically when they are placed at the point of signal entrance (antenna input) to the equipment.

Fortunately, one filter type, not as widely known as the more common R-C/L-C types, can be quite effective for the lower band RF noise. It is the *common-mode choke*, which can be designed for effective interference filtering at frequencies below 100 kHz, but with minimal impact on normal audio signals. Shown below in simplified form with a balanced-input preamp, a common-mode choke is a tightly coupled and somewhat specialized transformer (for audio use); it is typically wound with bifilar wire. A detailed technical analysis of CM choke operation can be found in [B2]; this discussion focuses on the practical implications for high-quality audio stages. The trifilar-wound CM chokes described by Gelbach [B3,B4] operate on similar principles, in dc and LF instrumentation.



Most interfering signals picked up on audio signal lines appear to the receiving circuit as CM signals, or at least predominantly CM. Therefore, for high rejection of CM signals in cases of extreme high level, high frequency inputs or RF contamination, a single common-mode choke in series with differential amplifier inputs can be a very effective RFI solution.

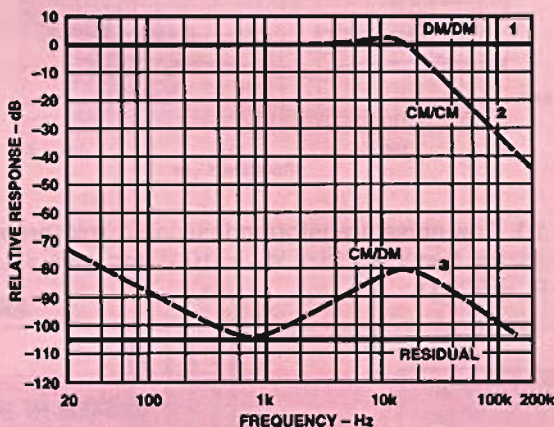
Perhaps the most important point to understand about CM chokes is that their behavior is distinctly different for signals applied in CM fashion, compared to the desired differential-mode (DM) signals. Because of tight flux coupling in the common core, CM signals see the full rated inductance of the choke, which works in conjunction with the balanced capacitive termination to provide a two-pole low-pass filter for these signals.

On the other hand, the DM signals do not see this high inductance, because their flux cancels. As a result, they only see the leakage inductance, and the higher associated bandwidth. Thus the DM and CM filter bandwidths of a high quality CM choke can indeed be quite different. It is this characteristic that allows the CM choke to pass full audio-range bandwidths without attenuation, while suppressing CM signals beginning just above (or actually within) the audio band. In addition, this

type of L-C filtering introduces little if any noise degradation to the signal, as long as the choke's dc resistance is of the order of 10  $\Omega$  or less.

The utility of CM filtering applies not only to microphone and other low-level circuits; it can also apply to higher-level line receiver circuits and A/D inputs as well. David Birt [B5] and Allen Burdick [B6] have described CM choke filtering techniques, like those outlined above, aimed specifically at audio circuits. CM filter circuitry can be inserted within a preamp proper, and/or used externally, as a packaged device, with standard XLR connector interfaces ahead of noise-susceptible gear. If used within a preamp, the network values of the filter would be optimized to complement the preamp input impedances. For wide bandwidth LF & HF filtering, cascaded chokes can be used. [B4]

The Benchmark Media Systems CMF-1 is an example of a two-pole CM filter in pre-packaged form; it is suitable for in-line use ahead of any preamp or line-level audio stage. In the figure below, its performance is shown in a 200-kHz bandwidth by log frequency response plots of: DM input/ DM output ("1"), CM input/CM output ("2"), and CM input/ DM output response ("3"), to 1-V rms signals (0 dB),  $R_L = 9.09$  k $\Omega$ . The normal signal DM passband is in excess of 200 kHz, while the CM passband is 26 kHz. The DM response to CM signals is below -80 dB or better at frequencies above 50 Hz, but the filter still has 60 dB of attenuation at 1 MHz (not shown). ▀



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\*Book available for purchase from Analog Devices. Use book purchase card.



## A/D Converters, Multiplexers, Codec

### +5-V Stereo Codec Has Serial Port


**AD1847 SoundPort® interfaces directly to DSPs**  
**Low-cost device is housed in 44-pin PLCC/TQFP**

The AD1847 is a monolithic low-cost 16-bit stereo codec for audio. Its flexible serial port interfaces directly to a DSP or system I/O chip. The device comprises key audio data-conversion and control functions, including stereo pairs of  $\Sigma$ - $\Delta$  A/D and D/A converters, programmable gain/attenuate/mute functions,  $\mu$ A-law compression and expansion, filtering, and a voltage reference. Two pairs of stereo line inputs are available at the input via a multiplexer; and two auxiliary pairs can be muxed to the input or mixed with the audio output.

Supporting the Microsoft Windows sound system, the AD1847 is a key element of a low-cost solution for business, game audio, and multimedia applications requiring operation from a single +5-V supply. The serial interface allows implementation on a computer mother-board, add-in, or

PCMCIA card. When used with a DSP, the AD1847 can support conversions for advanced audio capabilities, such as compression, spatial sound effects, and music synthesis.

Little off-chip support circuitry is needed. Anti-imaging output filters are included on-chip. Dynamic range exceeds 70 dB over the 20-kHz audio band. An on-chip oscillator, with external crystals, provides sample rates from 5.5 kHz to 48 kHz. The 16-bit output pair from the ADCs is available over a serial interface that also supports 16-bit digital input to the DACs, plus control/status information.


Specified for operation from 0 to +70°C, the device is housed in a 44-pin PLCC. With a +5-V supply, max power dissipation is 750 mW operating, 4 mW power-down. Price in 10,000s is well below \$10. **Circle 9** 

### Stereo 16-Bit ADC

**Single-supply  $\Sigma$ - $\Delta$  AD1877:**  
**92-dB SNR; 100  $\mu$ W “sleep”**

The AD1877 is a low-cost, +5-V 16-bit dual A/D converter on a single chip for audio-bandwidth applications. It includes a 2.25-V on-chip voltage reference, 4th-order 64 $\times$  oversampling  $\Sigma$ - $\Delta$  modulators, and 3-stage linear-phase decimation filters; its outputs are available via a serial output interface having 8 user-defined modes, both master and slave.


Performance features include 92-dB dynamic range (90-dB min), 20 Hz to 20 kHz (without A-weighted filtering) and 90-dB signal-to-noise-plus-distortion (88 dB min). Input overrange indication is provided, and power dissipation is low—315 mW max operating, 325  $\mu$ W max power-down while clocked (and a mere 5  $\mu$ W unlocked).

It is housed in a 28-pin SOIC, and operates at temperatures from 0 to +70°C. Price is \$10 in 1000s. **Circle 10** 

### Dual $\Sigma$ - $\Delta$ Modulator

**5th-order ADMOD79 has**  
**103-dB dynamic range**


The ADMOD79 is a 2-channel differential-input modulator for high-performance  $\Sigma$ - $\Delta$  stereo A/D converters of up to 18-bit resolution. Its single-bit monotonic outputs are produced by fifth-order modulators with proprietary, patented noise shaping and an on-chip dc voltage reference. With a 3.072-MHz modulator clock and 64 $\times$  oversampling, it offers 103 dB of dynamic range over 20 kHz.

Sophisticated system designers use this key building block to construct high-performance A/D functions. Performance can be tailored to the application using an application-specific digital decimation filter—implemented either as a fixed function or by a programmable DSP—and by an analog front end to match the input source to the modulator. Using  $\pm$ 5-V supplies, and housed in a 28-pin cerdip, the ADMOD79 operates from 0 to +70°C. Price is \$25 in 1000s. **Circle 11** 

### 10-Bit 20-MSPS ADC

**MIL-qualified AD773A**  
**S/(N+D)  $\geq$  51-dB @ 10 MHz**

The AD773A A/D converter is an improved direct replacement for the 10-bit, 18-MSPS AD773, introduced here 3 years ago (A-D 25-2, p. 14). It is available for both commercial and military (/883) temperature ranges, requires 300-mW less power (1.2 W max), has 8-dB less THD at 10 MHz (-55 dB max, K version). Its full-power input bandwidth is 100 MHz. Typical applications include infrared imaging, radar and communications, and applications in space/radiation environments.


Other features include no-missing-codes, guaranteed; high-impedance ( $\geq$ 50 k $\Omega$ ) reference input (2.5 V); out-of-range output flag; output available in binary and twos complement coding. The AD773A is housed in a 28-pin ceramic DIP and is available for 0 to 70°C and -55 to +125°C operation. Prices start at \$55 in 100s. **Circle 12** 

### Analog MUXes

**16-channel ADG406/426,**  
**Dual-8-channel ADG407**

The ADG406 and ADG426 are 16-channel CMOS multiplexers; the ADG407 is differential with 8-channels. The ADG426 has on-chip address and control latches; the ADG406/407 require external latches for microprocessor interfacing.

The devices will work with single- or dual supplies. The signal range for all three extends to the supply rails, and switching action is “break-before-make.”  $R_{ON}$  is 80  $\Omega$  max, and switching is fast (<160 ns  $t_{ON}$ , <150 ns  $t_{OFF}$ ). Power requirements are 5  $\mu$ A max  $I_{DD}$ ,  $V_{EN} = 0$ ; 500  $\mu$ A max,  $V_{EN} = 2.4$  V.

They are available in DIPs and PLCCs; and the ADG426 is the first latchable 16-channel MUX to be available in an SSOP package. They are currently available for the extended industrial (-40 to +85°C) temperature range. Prices (100s) start at \$6.25 (ADG406/407) and \$6.65 (ADG426). **Circle 13** 

*All brand or product names mentioned are trademarks or registered trademarks of their respective holders.*



## D/A Converters, Analog Switches

### Fast 16-Bit DAC

**DAC16 has current output & 500-ns settling, is monotonic**

The DAC16 is a high-speed parallel-input, current-output 16-bit D/A converter characterized by low noise (0.3 LSB max), low nonlinearity ( $\pm 1$ -LSB max differential nonlinearity), and low drift (0.025 ppm/ $^{\circ}$ C zero, 5 ppm/ $^{\circ}$ C gain). Its combination of fast (500-ns) settling and high dc accuracy make it well-suited for generating precise levels at high speed for control and test.

Typical high-speed, high-accuracy applications include waveform synthesis and modulation in equipment for communications, control, instrumentation, automatic test, and graphic displays.

TTL and CMOS-compatible, the DAC-16 is available in 24-pin plastic DIPs & SOL for the  $-40$  to  $+85^{\circ}$ C range, and ceramic DIPs & LCCs for  $-55$  to  $+125^{\circ}$ C; an evaluation board is available. DAC16 prices start at \$25 in 100s. **Circle 14** ▶

### Dual 12-Bit DAC

**Single-supply AD8582 Has rail-to-rail outputs**

The AD8582, operating on a  $+5$ -V supply, is a complete, adjustment-free parallel-input, dual 12-bit DAC with a rail-to-rail voltage output. It includes an on-chip laser-trimmed 2.5-V bandgap voltage reference and double-buffered data interface logic. It is essentially a dual-channel version of the DAC8562, introduced here last year (*Analog Dialogue* 27-1, p. 25). Typical applications include digitally controlled calibration, portable equipment, digitized servo and process controls, and power-level adjustment in communication equipment.

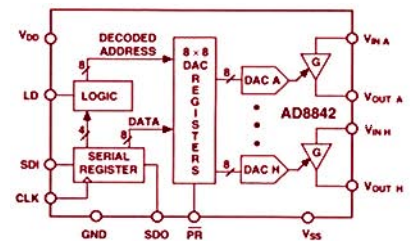
Its output is coded for convenient 1 mV/bit scaling (4.095 V for all-1s). Power dissipation is very low, typically 5 mW, ideal for battery-operated systems. Housed in PDIP-24 and SOL-24 packages, it has an operating temperature range of  $-40$  to  $+85^{\circ}$ C. Prices start at \$9.44 in 1000s. **Circle 16** ▶

### 8 $\times$ 8-Bit Multiplying TrimDAC®

**AD8842 has 8 independent gain-control channels, Serial input, flexible 4-quadrant multiplication**

A TrimDAC® provides low-cost digitally controlled adjustment of parameters in analog circuits, permitting designs that supplant manual or servoed pots. The AD8842 is a low-cost TrimDAC offering eight independent channels of four-quadrant-multiplying gain control. "Four quadrant" means that the controlled ac or dc signals can be unipolar or bipolar, and the range of gain adjustment includes both positive and negative gains.

The AD8842 contains eight independent voltage-input, voltage-output multiplying D/A converters, each having a bandwidth from dc to 50 kHz. Typical applications include vertical amplitude adjustment in CRT-based computer graphic displays, dc setpoint control of video amplifiers, automatic calibration, and waveform generation and modulation.



The digital gain-control input arrives on a standard 3-wire serial interface as a 12-bit serial word; 8-bit data is latched into one of eight DAC registers selected by the first four bits. A serial data output pin allows multiple DACs to be daisy-chained.

The AD8842 consumes 95 mW from  $\pm 5$ -V power supplies. It is available in 24-pin plastic DIP and SOL-24 packages, for operation at temperatures from  $-40$  to  $+85^{\circ}$ C. Prices start at \$5.69 in 1000s. **Circle 15** ▶

### 8 $\times$ 12-Bit DACPORT

**AD75089 is small, accurate Has readback and 0 reset**

The monolithic AD75089 DACPORT® comprises 8 channels of 12-bit voltage-output D/A conversion, complete with a  $+5$ -volt reference, output amplifiers, and double-buffered 12-bit parallel input. The buffer structure provides the ability to read back the value stored in a selected DAC latch and to reset all DAC latches to the most-negative value. Typical applications for multiple analog outputs include control systems, automatic test, and robotics.

With  $\pm 12$ -volt supplies, the analog output range is  $\pm 5$  V, with offset-binary coding. Max differential and integral nonlinearity specs are  $\pm 1/2$  LSB and  $\pm 1$  LSB at  $25^{\circ}$ C. The output slew rate is 3 V/ $\mu$ s, with  $\pm$  full-scale settling time of 8  $\mu$ s to  $\pm 1/2$  LSB. The device is housed in a 44-pin PLCC and has an operating temperature range of 0 to  $+70^{\circ}$ C. Price is \$76 in 100s. **Circle 17** ▶

### Quad SPST Switches

**Latchup-proof ADG441/2/4 -40 to +85°C in plastic**

The monolithic ADG441/42/44 comprise four channels of independently selectable single-pole, single-throw (SPST) CMOS switches. A trench isolation process provides latchup-proof rail-to-rail operation with single- or dual supplies. Compatible with existing 441/42/44 switches, they can improve performance of circuits using the ADG201A/02A/11A.

The ADG441 and ADG444 switches turn on with logic Low; the ADG442 switches with logic High. The ADG441/42 generate internal logic levels; the lower-cost ADG444 requires an external  $V_L$ . Switches are break-before-make and conduct equally well in both directions.  $R_{ON}$  is  $< 70 \Omega$ , with 3- $\Omega$  matching;  $t_{ON}$  is  $< 110$  ns and  $t_{OFF}$   $< 60$  ns. They are available for  $-40$  to  $+85^{\circ}$ C in 16-pin plastic DIPs and SOIC, and for  $-55$  to  $+125^{\circ}$ C in cerdip. Prices (100s) start at \$2.05/\$2.05/\$1.33. **Circle 18** ▶

## Op Amps & Analog Multiplier

### Rail-to-Rail Dual and Quad Op Amps

**OP291 and OP491: +3 to +10-V single supply  
Inputs swing  $V_s \pm 5$  V without phase reversal**

The OP291 and OP491 are single-supply dual and quad op amps that handle rail-to-rail inputs and furnish rail-to-rail outputs. As amplifiers tend to be used in applications requiring both lower supply voltage and less quiescent power, good dynamic range requires that the input and output signal swing over the whole supply-voltage range. These amplifiers will swing to within 50 mV of the + rail and 10 mV of the - rail (100-k $\Omega$  load).

When handling rail-to-rail signals, it is also important that the input can be driven at or beyond the supply voltage with simple clipping, i.e., without reversal of phase or latchup. The OP291 & OP491's amplifiers can be overdriven by up to 5 V beyond the supplies without latchup or phase reversal. This allows the designer to design with minimal—if any—input protection for almost all applications.

### 200 MHz TransZamp AD8015 meets 155-Mbps- fiber BW, noise, sensitivity

The AD8015 is a wideband (200 MHz) transimpedance amplifier optimized for use in fiberoptic receiver circuits with NRZ data rates up to 300 Mbps. It can be used in FDDI receivers and for SONET/SDH data rates up to 155.52 Mbps. An alternative to GaAs-based transZ amps, it is a complete solution for converting photodiode current input into a voltage output; its differential outputs can interface directly to ECL comparators or post-amps.

Specifications include 1.5-ns rise- and fall times; noise of 2 pA/ $\sqrt{\text{Hz}}$  at 100 MHz, (total rms of 20 nA in 100-MHz BW); optical sensitivity of -36 dBm at 155.52 Mbps, with peak input current of  $\pm 200$   $\mu\text{A}$ . The AD8015 uses a single +5-V supply, and needs only 25 mA. Housed in an 8-lead plastic SOIC, it operates from -40 to +85°C. Price (1000s) is \$3.59. Phone (617) 937-1124 ■

The OP291 and OP491 can operate at supply voltages from +2.7 V to +12 V. They require a maximum of 500  $\mu\text{A}$  per channel over the entire -40 to +125°C temperature range. DC specifications include 25 V/mV minimum open-loop gain, 1.5 mV max offset voltage and 60 nA max bias current over temperature. Noise is 2 mV p-p (0.1 to 10 Hz), 35 nV/ $\sqrt{\text{Hz}}$  at 1 kHz, and 0.8 pA/ $\sqrt{\text{Hz}}$ .

Dynamically, typical slew rate is  $\pm 0.4$  V/ $\mu\text{s}$ , small-signal gain-bandwidth is 3 MHz, full-power bandwidth is 1.2 kHz, and settling time to 0.01% is 22  $\mu\text{s}$ . Channel separation is 145 dB. They will drive a minimum short-circuit current of  $\pm 9$  mA.

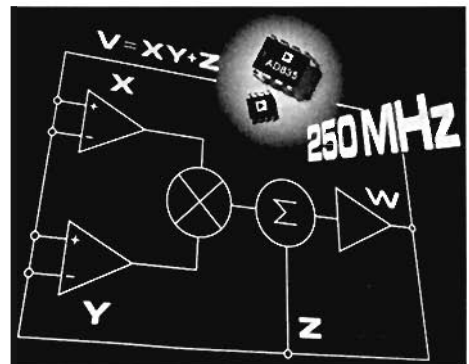
The OP291 is available in 8-lead mini-DIP and SO, and the OP491 is housed in a 14-lead epoxy DIP or 14-lead SO. Prices in 1000s start at \$2.16 for the OP291 and \$3.23 for the OP491. Circle 19 ■

### OP176 Audio Op Amp Dynamic range of bipolars, JFET speed & sound quality

The OP176 is a low-noise (6 nV/ $\sqrt{\text{Hz}}$ ), high-output-drive op amp with a Butler front end, efficiently combining the low noise and distortion of bipolar transistors with the speed and sound quality of JFETs. With its wide output range and short-circuit protection, it is an excellent choice for output sections of audio systems, driving lines and cables. The output is capable of driving 600- $\Omega$  loads to 10 V rms, while maintaining low noise and distortion (0.001% at 3 V rms).

The OP176 draws only 2.5 mA of supply current. Specifications include low dc offset (1.25 mV max, -40 to +85°C)—which permits adjustment-free circuits in many applications; wide bandwidth (10 MHz) and high slew rate (15 V/ $\mu\text{s}$ ); and it is unity-gain stable. It is packaged in 8-pin PDIPs and SOICs. Price starts at \$0.88 (88¢) in 1000s. Circle 21 ■

### 250-MHz Multiplier Vout, 4-quadrant AD835 8-pin miniDIP or SOIC



The AD835 is the industry's first monolithic 250-MHz, 4-quadrant voltage-output analog multiplier. It multiplies two single-polarity or bipolar differential input voltages (X and Y) and provides the true instant-by-instant product, with correct polarity, at the output. An additional summing input (Z) allows the output to be offset or compared with a reference (i.e., XY + Z).

It has low output impedance and high input impedance (100 k $\Omega$  || 2 pF). With  $\pm 5$ -volt supplies, its output range is  $\pm 2.0$  V min into 150  $\Omega$  over the -40 to +85°C temperature range; and it can drive load resistance as low as 25  $\Omega$ . It has a bandwidth of dc to 250 MHz (-3 dB), settles to within 0.1% of FS in 20 ns, and has a rise/fall time of 2.5 ns (1 ns for small signals). Its gain is flat to within -0.1 dB for frequencies up to 15 MHz. Nonlinearity (relative error) is within  $\pm 1\%$  of full scale and noise is only 50 nV/ $\sqrt{\text{Hz}}$  at 10 MHz.

Though its speed is state-of-the-art, the AD835 is easy to use; and its differential inputs and post-multiplication Z input provide added versatility. Besides very fast multiplication, division, squaring, & frequency doubling, it also provides wideband modulation and demodulation, and is useful in phase detection & measurement, video gain control & keying, and voltage-controlled amplifiers & filters.

Packages include 8-pin PDIP and SOIC. Price (100s) is \$8.95. Circle 20 ■



## Interfaces, Regulator, Temperature Sensor

### Vout Temp Sensor AD22100: -50 to +150°C On-chip signal conditioning

The AD22100 is a monolithic 3-terminal single-supply temperature sensor with on-chip signal conditioning and low-impedance voltage output proportional to the supply (22.5 mV/°C with a +5-V supply). Its 200° span is useful in many applications, including automotive, computer, instrumentation, and HVAC.

Its patented circuit measures and conditions the voltage developed across a temperature-sensitive resistor with constant-current excitation. Its ratiometric, rail-to-rail output provides a cost-effective solution with an A/D converter, using the ADC's reference as the AD22100's supply. Accuracy and linearity are better than ±2% & ±1% of full scale. Housed in a plastic TO92 package, it offers 3 ranges of measurement, **S**: -50 to +150°C, **A**: -40 to +85°C, and **K**: 0 to +100°C. Price (100s) starts at \$1.21. **Circle 22** ■

### S/R Isolated Interface AD2S75: Synchro/Resolver- to-system, X'former-coupled

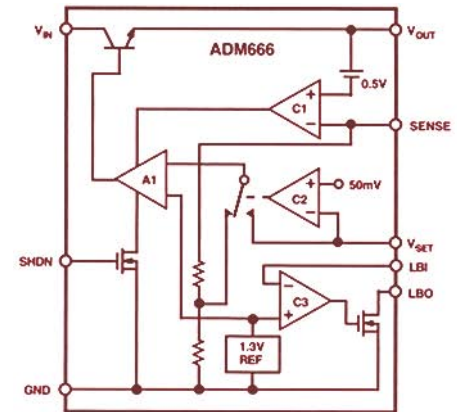
The AD2S75 is a universal transformer-isolated input interface between synchros & resolvers and conversion & conditioning circuitry. The AD2S75 can be pin-programmed to interface with all standard synchro- and resolver-format signals (90, 26, and 11.8 V rms) and produces outputs in sin-cos resolver format at a standard 2 V rms level. It operates over a range of reference frequencies from 60 Hz to 20 kHz.

The AD2S75's miniature transformers provide true galvanic isolation for up to 1000 volts dc. Applications include military systems & equipment, avionics, factory automation. Power input range is ±5 to ±15 V dc. It is housed in a hermetically sealed 24-pin, 0.9" DIP package and is available in industrial and military temperature ranges. Prices start at \$270 in 100s. **Circle 24** ■

### +5-V Linear Voltage Regulators ADM663 and ADM666 have existing 2nd sources Provide fixed +5 V or adjustable +1.3 V to +16 V

The ADM663 and ADM666 are complete precision voltage regulators that provide a fixed +5-volt output.\* With two additional external resistors, they provide a range of precision voltages from +1.3 to +16.0 V. Low quiescent current (12 µA max) makes them especially suitable for battery-powered systems. They will operate over an input range of +2 V to +16.5 V and can provide 40 mA of output current (more, if needed, using the AD663, via an external pass transistor). The AD663 also has a temperature-proportional output for use in powering liquid-crystal displays.

The **AD666** features battery-monitoring circuitry to detect low battery voltage. These devices are pin-compatible replacements for existing 663 and 666 regulators. Typical applications include battery-operated \*3-volt versions are also available. Ask about ADM663A and ADM666A. ■

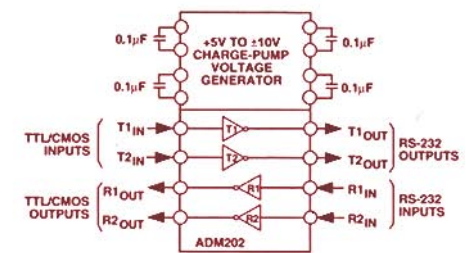


equipment such as notebook PCs, pagers, etc. Both devices are available in 8-pin plastic DIPs and narrow surface-mount SOIC packages. Their operating temperature range is -40 to +85°C. Prices (1000s) start at \$1.40 for the ADM663 and \$1.65 for the ADM666. **Circle 23** ■

### RS-232 Dual Transceivers, C = 0.1 µF ADM2x2 series have existing 2nd sources, Guarantee improved data rates up to 200 kb/s

The device types described here, ADM202, ADM222, ADM232A, and ADM242 are BiCMOS 5-volt dual RS-232 transceivers, which interface between the TTL processor bus (0 to 5 V) and ±5-V RS-232 lines (two channels in each direction); their internal charge-pump supplies employ compact 0.1-µF external capacitors.

These devices are improved pin-for-pin replacements to fit new and existing sockets. For example, the **ADM222**, **ADM232A**, and **ADM242**, operating from -40 to +85°C, guarantee a 200 kb/s data rate, a significant improvement over the 116 kb/s of existing 232A devices. The **ADM222** provides the 232A function, plus a shutdown capability (both transmit and receive) to reduce the supply current from 8 mA max to 10 µA max (0.1 µA typical). The **ADM242** includes both a shutdown capability (transmitters



only) and an Enable function for the receivers. The **ADM202** performs 232A functions at 0 to 70°C, draws only 4 mA max, and guarantees a 120 kb/s data rate.

The ADM202 and ADM232A are available in 16-pin plastic DIPs and SOICs; the ADM222 and 242 are housed in 18-pin DIPs and wide SOICs. In 1000s, the ADM202 is priced at \$1.20; the ADM222, ADM242, and ADM232A are priced at \$1.50. **Circle 25** ■

# A Reader Notes

## HIGH-FREQUENCY SIGNAL CONTAMINATION

by Leroy D. Cordill\*

I found your article on high-frequency signal contamination ("Ask The Application Engineer—14," *Analog Dialogue* 27-2, 1993) interesting and would like to offer some additional comments.

EMI/EMC requirements are becoming more important to designers of industrial equipment as analog signal sensitivities are increased while more "RF generators" (higher-frequency digital circuits) are incorporated into the same equipment. Therefore, I would like to see a *good* application note relating to the issue of RF susceptibility produced by someone such as Analog Devices. By "good", I feel it should cover:

- a. rules of thumb about the types of circuits where you will likely have trouble
- b. some explanation of the phenomenon
- c. general grounding/shielding approaches for equipment
- d. "fix" type approaches to minimizing the effects when items from (c) can't be implemented
- e. bench-level testing techniques.

(At least I'm not aware of any such application note in existence; maybe one exists and I haven't found it.) Based on my own experience, I offer the following comments on the above five areas:

Regarding (a), I generally see the problem with low-level input or preamp circuits involving a voltage gain of 50 V/V or more. In my case, the signals are usually from thermocouples, RTDs, pressure sensors, etc., and the required signal bandwidth is less than 100 Hz. And I'm trying to maintain signal integrity suitable for conversion by a 10-to-14-bit A/D converter.

For (b), my "model" of the effect is that the error gets created by rectification of the rf at the base-emitter junctions at the inputs of the op amp, and essentially becomes a large input offset voltage for the op amp. This introduces errors into dc-coupled circuits that cannot be corrected for by any usual low-pass filtering of the signal.

One observation I have made regarding this susceptibility problem is that it is primarily related to bipolar-type op amps (741, 5558, OP05, OP07, OP27, AD708, OP220, etc.) If I swap to a FET-input op amp (TL082, TL032, OP80, OP42, AD845) the error will largely disappear. (Due to other considerations, this is not usually a permanent solution, but helps to identify error sources during EMC testing.)

Also involved is the RF impedance at the two input nodes of the op amp. If (in a typical inverting configuration) the feedback path has a capacitor for low-pass filtering, it aggravates the problem as one input node of the op amp sees more of the RF than the other. If this is the situation, I'm not sure a wide-bandwidth op amp would help (regarding suggestions for using an AD830). Even without an intentional discrete capacitor in the feedback loop, PC-board layout makes it difficult to count on matched impedances at the two inputs.

\*RR 3 Box 8910, Bartlesville OK 74003. Leroy Cordill, a design engineer with Applied Automation, Inc., has been involved in designing process gas chromatographs for about 20 years. His areas of design have included system architecture, analog, digital, and serial communication circuits, as well as GC detectors and valves.

†See Book Purchase card.

Regarding (c), a good RF ground to the chassis is important for the signal common; but I find the shielding/grounding aspects of the equipment design relate more to the ESD requirements than RF (continuous-wave) susceptibility problems. I also try not to rely on these (shielding/grounding) to a great extent, since I find them very uncontrollable during the life of a piece of field-customizable equipment.

For (d), my best, most consistent prescription is placing a small capacitor directly across the input pins on bipolar op amps. I have used 100-1000 pF for this purpose in various circuits; it usually significantly reduces or eliminates the problem up to the level of interference that I plan for. I have found that with this in place on the critical parts of the circuit, the requirements for extreme care in grounding and shielding of cables are greatly reduced.

Regarding (e), I agree that a small walkie-talkie is useful, but primarily as a go/no-go test on the equipment when it is all assembled, in the enclosure, etc. However, for pc board or circuit-level work, I have two problems with the walkie-talkie technique: (1) you will get many unkind remarks from the guy on the next bench over if he's trying to breadboard a low-level circuit and is not ready for EMI testing yet; and (2) if you start attaching leads to various points in the circuit to determine where the problems are, and then apply RF in a radiated fashion, you have so many antennae, both to your circuit and to the various test gear, that you will have *no* idea what is happening.

I prefer to use an RF signal generator and apply the interference in a conducted fashion. This allows much better control of which items get RF applied to them. I don't use a lot of RF power, as I usually connect the output of the generator directly to some connector or cable supplying the low-level signal of interest, or in some cases the body of a sensor. A few hundred millivolts of RF signal is generally sufficient to identify problem circuits. I manually sweep from about 10 MHz to 100 MHz. While this is not a quantitative type of test, it is a very useful qualitative technique.

Some of the RF generators I have used for this are older model units—usually acquired at garage sales for \$5 to \$20 each:

- RCA WV-50B
- Advance Schools, Inc., Model IGB-102
- Heathkit Model IG-102 (same as above)
- Precise Model 630

I hope this may be useful, and, as I mentioned would like to see a good application note put together on this subject by someone who can add some additional information regarding performance implications of adding a capacitor on the op-amp inputs for various circuit configurations.

*Thanks to Mr. Cordill for a useful contribution to the Dialogue, and for throwing down the gauntlet to our Application Engineers. They have accepted the challenge; so keep your eyes on the "Worth Reading" page in future issues. Having said that, we feel obliged to point out that the challenge is to get it together in one place; much of the material he suggests already exists in the Analog Devices literature (and elsewhere). For example, see p. 17 of this issue. Also, the System Applications Guide† devotes pages 1-13 thru 1-55 to remote sensor application problems—including an exhaustive discussion of RFI rectification in high-accuracy circuits. Other good sources include the Applications Reference Manual,† Chapter 3 and Bibliography of the Transducer Interfacing Handbook,† and Part 5 and Bibliography of the Analog-Digital Conversion Handbook.†*



# Ask The Applications Engineer—16

by Oli Josefsson

## USING SIGMA-DELTA CONVERTERS—PART 2

*This is a continuation of a discussion of sigma-delta converters begun in the last issue. We covered antialiasing requirements, idle tones, and loading on the signal source.*

**Q:** *What happens if my input signal is beyond the input range of the sigma-delta converter? I remember hearing something about the converter becoming unstable?*

**A:** The modulator can become temporarily unstable if it is driven with inputs outside the recommended range. However, this instability is invisible to the user, since decimators are designed to simply clip the digital output and show either negative or positive full scale, just as one would expect with a conventional converter.

**Q:** *The specifications for sigma-delta converters assume a certain input clock rate and therefore a specific sampling rate. Can I safely use the converter with a higher or lower clock frequency?*

**A:** While the specs are measured at a particular sampling frequency, we often specify a range of input clock frequencies that the device can be operated with. This translates into a range of possible sampling rates. If you plan to go much beyond that range you can expect some performance degradation. If you sample at higher rates than specified, the internal switched-capacitor circuits may not be able to settle to the required accuracy before a new clock edge comes along. With too slow a sampling rate, capacitor leakage will degrade performance.

The digital filter characteristics of the converter (group delay, cutoff frequency, etc.) scale with sampling rate; so too do the input impedance (unless the input is buffered) and power consumption.

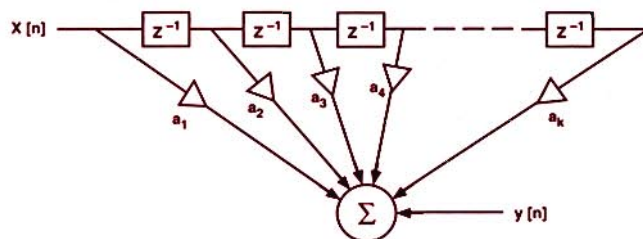
**Q:** *I am planning to use a sigma-delta converter to digitize several signals by using a multiplexer at the input of the converter. Is that a problem?*

**A:** While sigma-delta converters have a certain appeal due to their ease of antialiasing, they do not lend themselves well to applications for multiplexed ac signals. The reason for this is that the output of a sigma-delta converter is a function not only of the latest analog input but also of previous inputs. This is mostly due to the memory that the digital filter has of previous inputs, but the modulator has some memory as well. In a multiplexing application, after switching from one input to another, all information the filter has about the old input needs to be flushed out before the converter output word represents the new input.

Most decimation filters in sigma-delta converters intended for ac applications are FIR filters, principally because of their linear phase-response. For FIR filters, it is easy to calculate the time it takes to rid the filter of any information about the old input. The figure shows the structure of a FIR filter; the number of clock cycles required to clock all old data points out (i.e., the filter settling time) is equal to  $k$ , the number of taps in the filter. While data corresponding to a new input is propagating through the filter and replacing the earlier data, the output of the filter is calculated from a combination of the old data and the new data. The AD1879, for example, an 18-bit audio A/D

converter, has a 4096-tap FIR filter which, when running at 3.072 MHz, has a 1.33-ms settling time.

The effective sampling rate for sigma-delta converters in multiplexed applications is quite low because of this need to wait for the old signal to be flushed out before capturing a valid data point for the new input. Traditional converters, which convert directly, or in a small number of stages, are therefore a much better choice in applications requiring the capture of multiple ac channels.



$$y(n) = a_1 x(n) + a_2 x(n-1) + a_3 x(n-2) + \dots + a_k x(n-k+1)$$

For a multichannel dc application where time is available to wait after switching between channels, or if the application does not require frequent changes between channels, the use of a sigma-delta converter can be very feasible. In fact, Analog Devices offers 16-24-bit converters with multiplexers on the input (AD771x family) specifically for such applications.

**Q:** *Does this also explain why sigma-delta converters are not suitable for some control applications?*

**A:** Yes. Since delays in control loops must be minimized for stability, sigma-delta converters are not suitable for control applications where they add a relatively long time delay. However, the actual delay is predictable; in applications that involve relatively slow signals, the converter phase delay, and therefore the effect on pole and zero locations of the control loop, may be negligible. However, even if this is the case, a traditional non-oversampling converter may still be a much better choice for the application, because a sigma-delta converter would need to run at a much faster sampling rate than a traditional converter in order to have the same phase delay. This will unnecessarily burden the circuitry that processes the A/D data.

**Q:** *Are there any other issues I should be aware of when using sigma-delta converters?*

**A:** In addition to the general guidelines on grounding, power supply bypassing, etc., that apply to all converters, there are a couple of points worth remembering when designing with sigma-delta converters. The first issue involves their input. As mentioned earlier, some sigma-delta converters (such as the AD1877) have buffers on the input; others (such as the AD1879), without a buffer, present a switched-capacitor load, which needs periodic current transients to charge the input capacitor. It is important that the circuitry driving the converter be as close to the converter as possible to minimize the inductance in the leads between the external circuitry and the switched-capacitor node. This reduces the settling time of the

input and minimizes radiation from the input to other parts of the circuit board.

Another issue has to do with interference from clock signals affecting the A/D conversion. As I noted earlier, the digital decimation filter can't provide any filtering of signals whose frequencies are close to multiples of the modulator sampling rate. To be precise, the passbands are  $[kF_{ms} \pm f_b]$ s where  $k$  is an integer,  $F_{ms}$  is the modulator sampling rate, and  $f_b$  is the decimator cutoff frequency.

Besides the consequences for anti-aliasing discussed earlier, the decimator cutoff frequencies have a bearing on the selection of clock frequencies for devices that operate in the same system as the converter. These frequency bands (i.e., the passbands) embody the converter's greatest vulnerability to interference (inductive or capacitive coupling, power supply noise, etc.), because any signals in these frequency bands that manage to get into the modulator will not be subjected to attenuation in the filter. Therefore one is wise to avoid using clock frequencies that fall in these bands to minimize the possibility of interfering with the conversion—unless they are synchronous with the converter clock.

### QUESTIONS ON NOISE IN CONVERTERS

*Q: I recently evaluated a dual-supply A/D converter; one of the tests I did was to ground the input and look at the output codes on a LED register. To my big surprise I got a range of output codes instead of a single code output as I expected?*

**A:** The cause is *circuit noise*. When the dc input is at the transition between two output codes, just a little circuit noise in even the finest dc converters will ensure that two codes will appear at the output. This is a fact of life in the converter world. In many instances, as in your case, the internal noise may be large enough to cause several output codes to appear. Consider, for example, a converter with peak-to-peak noise of just over 2 LSB. When the input of this converter is grounded, or a clean dc source is connected to the input, we will always see three—and sometimes even four—codes appear at the output. The circuit noise prevents the voltage being sampled from being confined to a voltage bin that corresponds to one digital code. Any external noise on the A/D input (including a noisy signal), on the power supplies, or on the control lines will add to the internal circuit noise—and possibly result in more bits toggling.

*Q: Is there a way to determine how many codes I can expect to appear when I apply a dc signal to a converter?*

**A:** It would not be hard in the ideal case where you knew the noise distribution, the exact size of the codes where the dc input is at and where within a code quantum the input lies (in the center, on the edge of two codes, etc.). But in reality you don't have this information. However, knowing some of the ac specifications (S/N, dynamic range, etc.) of the converter, you can make an *estimate*. From these specs you can find the magnitude of the rms converter noise relative to full scale. The noise will in all likelihood have a Gaussian amplitude distribution, so the standard deviation (sd) of the distribution equals the rms value. This also means that the codes that appear will not have equal probability of occurring. Using the fact that 99.7% of a Gaussian distribution occurs within  $\pm 3$  standard deviations from the mean, we can estimate the peak-to-peak noise voltage at six times the standard deviation.

If  $N_{rms}$  is the rms value of the converter noise and  $V_{LSB}$  is the size of the LSB in volts ( $= V_{span}/2^b$ ) the peak to peak noise in terms of LSBs,  $N_B$ , is

$$N_B = \frac{6 \times N_{rms}}{V_{LSB}} = \frac{6 \times 2^b \times N_{rms}}{V_{span}}$$

In general, if the signal-to-noise ratio of a converter expresses noise power relative to full scale, we have

$$N_B = \frac{3}{\sqrt{2}} \times 2^b \times 10^{-\text{SNR}/20}$$

where  $b$  is the number of bits in the output word.

How many codes show up at the output depends where the mean of the input, i.e., the dc input value, is with respect to code transitions. If the mean is close to the boundary between two output codes, more codes are likely to appear than if the mean is half way between two output codes. It can easily be shown that  $N_C$ , the number of codes appearing for a particular value of  $N_B$ , is either  $\text{INT}(N_B)+1$  or  $\text{INT}(N_B)+2$ , depending on the dc input value ( $\text{INT}(N_B)$  is the integer portion of  $N_B$ ). And don't be surprised to see even more codes from the less-probable noise amplitudes  $>\pm 3$  sd.

How many bits will  $N_C$  cause to toggle on the output? The number of bits needed to represent  $N_C$  codes is

$$\text{INT}\left(\frac{\log N_C}{\log 2} + 0.5\right)$$

We can, however, see many more bits toggle, since the number of bits toggling is a function of the actual value of the converter's dc input. Consider, for example, that a one-code transition from an output word of  $-1$  to  $0$  on a  $2s$ -complement-coded converter involves inverting all the output bits.

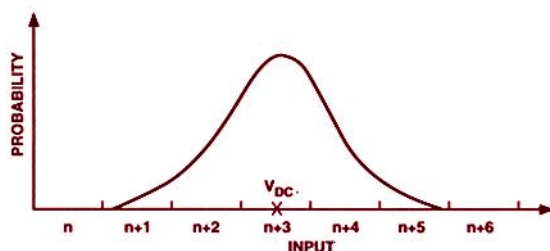
Lets look at an example using the AD1879, an 18-bit sigma-delta converter with dynamic range of 103 dB. From the definition of dynamic range we have

$$103 = 20 \log \frac{S}{N_{rms}}$$

From the AD1879 data sheet, we find that the rms value of a full-scale input signal,  $S$ , is  $6/\sqrt{2}$  V rms. This allows us to solve for  $N_{rms}$ , which turns out to be  $30 \mu\text{V}$ . We next find the LSB size by dividing the full input range by the number of possible output codes:

$$V_{LSB} = \frac{12}{2^{18}} = 45.8 \mu\text{V}$$

Thus  $N_B$  is 3.9. We can therefore expect either 4 or 5 different codes to appear at the AD1879 output when the input is grounded (ground corresponds to a midscale input for the AD1879).



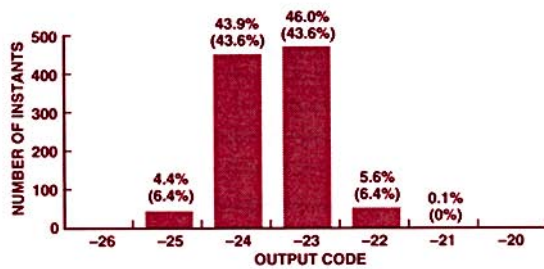
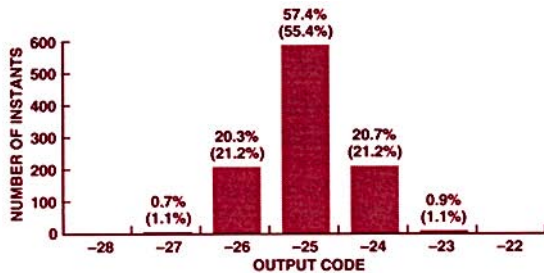


One can take this estimation one step further: If the standard deviation (the rms value) of a Gaussian distribution and the mean (the mean of the noise is 0 in this case) are known, one can use standard tables for the Gaussian distribution to calculate what percent of the time the noise will fall into a voltage interval corresponding to a specific output code. A histogram can be estimated, showing the distribution of codes at the output. Also the process can be reversed: a histogram showing the distribution of noise codes at a given value of dc output permits one to estimate the S/N ratio for a converter.

To make all this real, let's continue our example involving the AD1879. Consider two cases, one where the input lies midway between two output codes and one when the input is on the transition between two codes. From the calculations above, we found that the standard deviation (sd) of the noise (the rms value) was 30  $\mu\text{V}$ . The size of one LSB in terms of sd is

$$\frac{45.78 \mu\text{V}}{30.0 \mu\text{V}} = 1.524$$

In the case where the dc input is midway between code transitions, as shown below, it is clear that any noise that falls within  $-0.5$  LSBs to  $+0.5$  LSBs from the input will result in the correct code at the A/D output. This corresponds to the noise being confined to a range of  $(-0.5 \times 1.524)$  sd to  $(+0.5 \times 1.524)$  sd from its mean (0). From standard tables one can find that the noise will fall in this range 55.4% of the time. If the noise falls within 0.5 LSBs to 1.5 LSBs, the output will be one code too high. Again from standard tables one can find that this will occur 21.2% of the time. Continuing in this manner one can calculate the whole histogram showing the distribution of output codes.



The upper figure shows an actual measurement where the dc input happened to be  $-25$  LSBs. Five output codes, ranging from  $-27$  to  $-23$ , appeared. 1024 measurements were taken and the percentage distribution of each code is shown on top of each column. The calculated distribution is listed in brackets on top of each column. As can be seen, the experimental results agree well with the calculated values. The lower figure shows a case where the dc input is close to the boundary between two codes. By following a similar procedure, one can calculate how the histogram should look. Again the experimental and

calculated values are in excellent agreement. Note that the actual applied dc input is slightly above the border between the two codes, whereas the calculations assume it is exactly on the border.

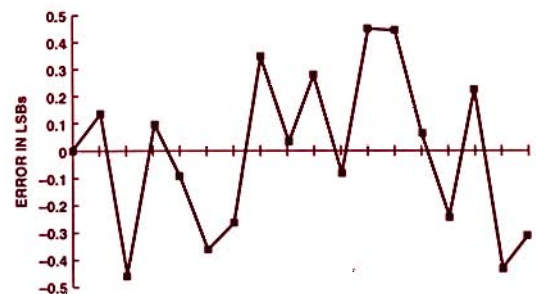
The biggest weakness of this estimating technique is the fact that in conventional converters the code width (the amount the dc input has to be increased to increase the digital output by one bit) varies from code to code. This means that if the dc input is in an area where codes are narrow, we can expect more bits to be toggling than in an area where the codes are wide. This method also assumes that the circuit noise within the converter stays constant, whether the applied signal is ac or dc. This is not exactly true in many cases.

The estimate will probably be more accurate when used with sigma-delta converters (except for "dead bands"), because neither of the two factors mentioned above is an issue in such converters.

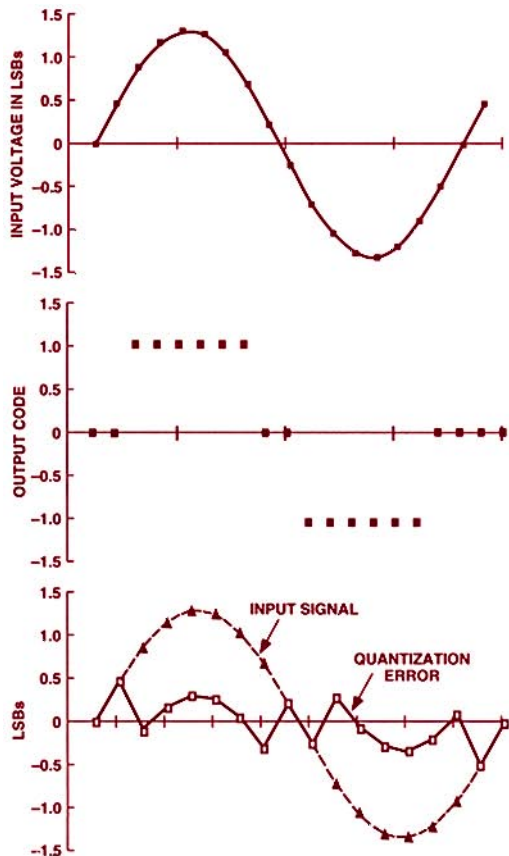
*Q: Ah, now I understand why there are multiple codes at the output. But why not discard the bits that toggle and only bring out the bits that stay steady, since the others are really indeterminate? Isn't that the real resolution of the converter?*

*A: Many converters are designed for ac or dynamic applications where THD (total harmonic distortion) and THD+N (total harmonic distortion+noise) are the most important specs. The design therefore focuses on minimizing harmonic distortion for high- and low-level input signals, while keeping the noise to acceptable levels. As it turns out, these requirements somewhat contradict the requirements for a good dc converter, which is optimized for precision conversion of slow moving signals where harmonic distortion is not an issue. It is actually desirable to have some noise (called dither) superimposed on the input signal to minimize distortion at very low input signal levels; dither can also be used to improve dc accuracy where repeated measurements can be made.*

To understand how this may be, let's start by looking at quantization noise. The output of an ideal A/D converter has finite accuracy because of the finite number of bits available to represent the input voltage. Each one of the  $2^b$  quanta represents with one single value all values in the analog range from  $-0.5$  LSB to  $+0.5$  LSB of its nominal input value. The A/D output can therefore be thought of as a discrete version of the analog input plus an error signal (quantization noise). When a large and varying input signal (dozens, hundreds, or thousands of LSBs in amplitude) is applied to a converter, the quantization noise has very little correlation with the input signal. It is, in other words, approximately white noise. The figure shows the quantization noise of a perfect A/D converter at various instants of time when the input signal is a sinusoid of about 100 LSBs in amplitude.



When the A/D input is very low in amplitude, so that the amplitude does not change more than a fraction of a LSB between samples, the samples stay in the same quantum, and are therefore constant for a few sample periods. This is depicted in the figure below, which shows a sinusoidal input signal that has an amplitude of only 1.5 LSBs, the A/D output and the quantization noise. Note that the quantization error follows the input waveform exactly while the samples are staying constant. The longer the samples stay constant, the more the quantization noise looks like the input waveform, i.e., the correlation between the input signal and the quantization noise increases. While the rms of the quantization error may not have changed, the quantization error will take on a non-uniform spectral shape. In fact, the correlated quantization noise shows up as harmonics in the A/D spectrum.

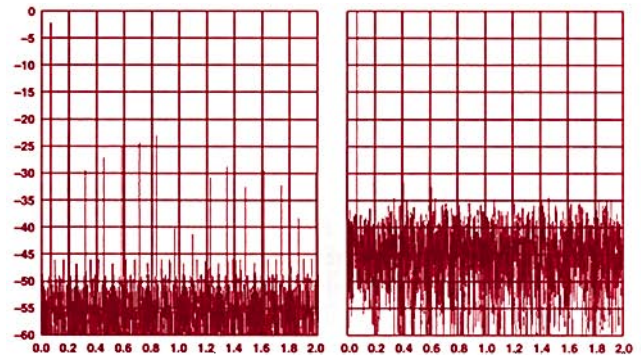


Another way to look at this phenomenon is to consider the case when the (sinusoidal) input signal is only around 1 LSB in size and the digital output resembles a square wave. Square waves are rich in harmonics! The harmonics, or noise modulation products, are very objectionable in many converter applications, especially audio.

To get around this problem, a technique called dithering is used to trade correlated quantization noise for white noise, which is less offensive to the human ear than correlated noise. Dithering is done by using circuit elements to *add* random noise to the input signal. While this will result in an increase of the total converter noise, the added noise breaks up the simple square wave patterns in the output code. The quantization error will not be a function of the input signal but of the instantaneous value of the dither noise. Thus the dither decorrelates the quantization noise and the input signal. The size of the dither

signal is often about 1/3 LSB rms (2 LSBs peak-to-peak if the noise is Gaussian). Clearly, this will result in a converter that will have more than two codes at the output when the input is grounded. We saw an example earlier involving the AD1879 which had either four or five codes appear on the output depending on the dc input level.

The figure below shows the simulated output of an A/D converter with an undithered low level input signal. The quantization noise is a function of the input signal magnitude at the sample instant. This correlation between the quantization noise and the input signal shows up as a cluster of harmonically related sticks in the A/D output spectrum. Note that the magnitude scale in the figure is referenced to the input signal (not full scale input).



The right-hand figure shows the A/D output after a dither signal that is 4 dB above the quantization noise floor is added to the input. In this case the quantization noise depends on the magnitude of the dither signal at the instant when a sample is taken. Since the value of the dither doesn't depend on the input signal, the quantization noise becomes uncorrelated to the input and the harmonics in the A/D spectrum are eliminated, but at the cost of an overall increase in the noise floor.

Instead of actually adding noise to the A/D input, dithering can be accomplished by using the thermal noise of the converter as the dither signal and calculating enough output bits to ensure a decorrelated quantization noise.

Though I have used A/D converters in my examples, the idea of using dither also applies to D/A converters as well. Dither is applied to D/A converters by adding the output of a digital noise generator to the digital word sent to the D/A.

*Q: But in dc applications, I want to make an accurate measurement each time and may not be able to tolerate the uncertainty of having a few LSBs of error in a particular measurement.*

*A: If you need n-bit dc accuracy in each conversion and you have problems finding a suitable n-bit converter, you have two options. One is to use an (n+2)-bit converter and simply ignore the two LSBs. However, if your hardware has the capability (and time) to do some signal processing, you can enhance the resolution of a noisy (dithered) dc converter and, in fact, get more than n-bit accuracy out of an n-bit converter if the accuracy is limited by noise.*

To understand why this may be so, think of an ideal n-bit converter. For a particular value of dc input, you will get one digital code at the output. However, you do not know where the input lies within the code quantum (i.e., in the middle,



close to the upper transition, etc.). That may be sufficiently accurate for your application, but if you add noise to the input of the converter—so that several codes can appear at the output—you will find that the code distribution contains information to place the dc value of the input more exactly.

In the earlier examples involving the AD1879, we saw how the code distribution looks when the input is in the vicinity of a code transition; the two most-frequent output codes are the ones on either side of the transition. Their average is therefore a good estimate of where the input lies. In fact, taking the average of a lot of conversions, while the input stays put, is an excellent way of enhancing the resolution of the converter. One has to be careful, when processing the converter output, to allow the output word length to grow without introducing roundoff errors. Otherwise one actually injects unwanted noise—called *requantization noise*—into the final output. Note that filtering out the noise is only just that; it will have no effect on other error sources of the converter, such as integral and differential nonlinearity.

This concept of resolution enhancement is an interesting one and is not restricted to the dc domain. One can actually trade resolution for bandwidth in the ac domain and combine the outputs of several converters or to construct a more-accurate output. The basic principle is that signal repetitions (which are self-correlated) add linearly, while repetitions of random noise produce root-square increases. Thus, a fourfold increase in number of samples increases S/N by 6 dB. Perhaps we can discuss useful applications of this principle in these pages in the future.

Q: You mentioned a couple of converter ac specifications above. I am somewhat confused about how SIN, THD+N, THD, S/THD, S/THD+N, and dynamic range are measured on A/D and D/A converters and how they relate to each other. Can you shed any light on this?

A: Your confusion is quite understandable. There is unfortunately no industry standard on exactly how these quantities are measured and therefore, what exactly they mean. Sometimes manufacturers are guilty of choosing the definition that portrays their part favorably.

Most often data sheets include a note on the testing conditions and how the different specs were calculated. The best advice I can give is to read these very carefully. By simple calculations you can often convert a specification for one part to a number that allows a fair comparison to a specification for another part.

Most specifications are not expressed in absolute units, but as relative measurements or ratios. Noise, for example, is not specified in rms volts, but as SNR, or the ratio between signal power and noise power under particular test conditions. These ratios are usually expressed in decibels, dB, and occasionally as percentages (%). A power ratio,  $x$ , expressed in bels, is defined as  $\log_{10}x$ ; multiply by 10 if expressed in decibels (one tenth of a bel):  $10 \log_{10}x$ . SNR is therefore equal to  $10 \log_{10}(\text{signal power/noise power})$  dB. Evaluated in terms of rms voltage quantities,  $SNR = 20 \log_{10}(V_{\text{signal}}/V_{\text{noise}})$ .

Armed with this knowledge, let's see whether we can make sense out of the multiple specifications you mentioned above (many of which are redundant). Those specifications seek to describe how the imperfections of the converter affect the

characteristics of an ac signal that gets processed by the converter. For dc applications, a listing of the magnitude of the actual imperfections suffices, but these can only suggest ac performance. For example, integral nonlinearity is a major factor in determining large-signal distortion (along with glitch energy for D/As) while differential nonlinearity governs small-signal distortion. To accurately determine the ac performance, at least two types of tests are performed in the case of A/Ds. The tests are as follows:

#### Full-scale sine (a)

A sinusoidal signal approaching full-scale is applied to the converter. The signal is large enough so that converter's imperfections cause significant harmonic components to occur at multiples of the input signal frequency. The harmonics will show up in the output spectrum, along with noise. A common performance measure is the relative magnitude of the harmonic components, usually expressed in dB. Relative to what? Two possibilities are the applied input signal and the full scale of the converter (which in most cases is different from the applied input signal). Referring the harmonics to full scale will clearly yield a lower (more attractive) number than referring them to the rms value of the actual input signal. This reference issue causes a lot of confusion when dynamic specifications are evaluated, because there is no universally accepted standard for what each performance measure should be referred to. The best advice I can give you is: never assume anything; read manufacturers' data sheets very carefully.

Sometimes the magnitudes of the individual harmonics are specified, but most often only the total harmonic distortion (THD) is specified. The THD measures the total power of the harmonics and is found by adding the individual harmonics in rms fashion. The formula then for THD when referred to the input signal is

$$20 \log_{10} \left[ \frac{\sqrt{\sum_{i=2}^m H^2(i)_{rms}}}{S} \right] \text{ or } 10 \log_{10} \left[ \frac{\sum_{i=2}^m H^2(i)_{rms}}{S^2} \right]$$

where  $H(i)_{rms}$  refers to the rms value of  $i$ th harmonic component and  $S$  to the rms value of the input signal. Usually, harmonics 2 through 5 are sufficient. Note that the input-frequency, or *fundamental*, component is the first harmonic. To refer any harmonic to full scale, add  $x$  dB to the formula above, where  $x$  is the magnitude of the input signal relative to full scale. This simple conversion formula can be applied to other specifications, but take care to observe proper polarity of the log quantities.

Nowadays, clear distinction is usually made between total harmonic distortion plus noise (*THD+N*) and *THD*. This has not always been the case. *THD+N* includes not only the harmonics that are generated in the conversion, but also the noise. The formula for *THD+N* when referred to the input signal is:

$$20 \log_{10} \left[ \frac{\sqrt{N^2_{rms} + \sum_{i=2}^m H^2(i)_{rms}}}{S} \right]$$

or

$$10 \log_{10} \left[ \frac{N^2_{rms} + \sum_{i=2}^m H^2(i)_{rms}}{S^2} \right]$$

where  $N_{rms}$  is the rms value of the integrated noise in the bandwidth specified for the measurement.

Another commonly used specification is signal to noise-plus-distortion ( $S/(N+D)$ , or  $S/(THD+N)$ ), also called *sinad*. This is essentially the inverse of  $THD+N$ , when referred to the signal; its dB number is the same, but with opposite polarity.

Another performance measure describing the test results is the signal to noise ratio,  $S/N$  or  $SNR$ , which is a measure of the relative noise power, most useful for estimating response to small signals in the absence of harmonics. If  $S/N$  is not specified, but  $THD$  and  $THD+N$  are provided, relative to the input signal,  $THD$  can be rss-subtracted from  $THD+N$  to obtain the noise to signal ratio [ $= 1/(S/N)$ ]. If the numbers are given in dB, the rss subtraction formula for logarithmic quantities in the Appendix can be used as follows

$$SNR = -10 \log_{10} \left( 10^{(THD+N)/10} - 10^{THD/10} \right)$$

to yield the input signal power relative to noise power expressed in dB.

#### Low-level sine (b)

The second test usually performed is to apply a sinusoidal signal well below full scale to the converter (usually -60 dB). At this input level, sigma-delta converters usually exhibit negligible nonlinearities, so only noise (no harmonic components) appears in the spectrum. At this level,  $S/N = S/(N+D) = -THD+N = -THD$ , when all are referred to the same level. As a result, one specification indicating the noise level suffices to describe the result of this test. This specification called *dynamic range* (inversely, *dynamic-range distortion*), specifies the magnitude of the integrated noise (and harmonics if they exist) over a specific bandwidth relative to full scale, when a -60-dB input signal is applied to the converter.

Conventional (i.e. not sigma-delta) converters can exhibit harmonics in their output spectrum even with low-level input signals because all the codes may not have equal width (differential nonlinearity). In some such instances, the  $S/N$ , which ignores harmonics, measured with a -60-dB input signal, is different from dynamic range.

Frequently one sees  $THD+N$  at -60-dB and dynamic range specified for the same converter. These really are, as explained above, redundant since they only differ in the reference used. The only twist on dynamic range is that sometimes, when audio converters are specified, a filter that mimics the frequency response of the human ear is applied to the converter output. This processing of the converter output is called A-weighting (because an A-weighting filter is used); it will effectively decrease the noise floor, and therefore increase the signal-to-noise ratio, if the noise is white.

Everything discussed above applies to both A/D and D/A converters, with the possible exception of signal to noise ratio. Sometimes (particularly for audio D/A converters)  $S/N$  is a measure of how "quiet" the D/A output is when zero (midscale) code is sent to the converter. Under these conditions, the  $S/N$  expresses the analog noise power at the D/A output relative to full scale output.

It's important to note that the performance measures above are affected by: *bandwidth* of the measurement, the *sampling frequency*, and the *input signal frequency*. For a fair comparison of two converters, one has to make sure that these test conditions are similar for both.

#### Another Question

**Q:** I intend to use Analog's AD1800 family of audio D/A converters for a digital audio playback application. I understand that using an interpolator ahead of the D/A will make it easier to filter the D/A output, assuming I want to get rid of all the images at the D/A output. But is it really necessary to filter the output, since all the images will be above the audible range as long as sampling is at >40 kHz.

**A:** Good question. The audio equipment (audio amplifiers, equalizers, power amplifiers, etc.) that may eventually receive the output of your D/As are typically built to handle 20-Hz to 20-kHz signals. Since they are not intended to respond at frequencies much beyond 20 kHz—and in effect themselves function as filters—they may not have the necessary slew rate and gain to handle incoming signals from an unfiltered D/A output having significant energy well above 20 kHz. With their slew-rate and gain limitations, the amplifiers are driven into nonlinear regions, generating distortion. These distortion products are not limited to high frequencies but can affect the 20-Hz to 20-kHz range as well. Attenuating the high frequency signals at the DAC will therefore reduce the possibility of distortion. CD players often include filters steep enough to reduce the total out-of-band energy to >80 dB below full scale.

#### APPENDIX

**RSS addition of logarithmic quantities:** The root-square sum of two rms signals,  $S_1$  and  $S_2$ , has an rms value of  $\sqrt{S_1^2 + S_2^2}$ . One often needs to calculate the rss sum of two numbers that are expressed in dB relative a given reference. To do this one has to take the antilogs, perform the rss addition, then convert the result back to dB. These three operations can be combined into one convenient formula: If  $D_1$  and  $D_2$  are ratios expressed in dB, their sum, expressed in dB, is

$$10 \log_{10} \left( 10^{D_1/10} + 10^{D_2/10} \right)$$

Similarly, to find the difference between two rms quantities,

$$x = \sqrt{S_2^2 - S_1^2}$$

the result,  $x$ , expressed in dB, is

$$10 \log_{10} \left( 10^{D_2/10} - 10^{D_1/10} \right)$$

#### References:

- [1] *Oversampling Delta-Sigma Data Converters—Theory, Design, and Simulation*, edited by J.C. Candy and G.C. Temes, IEEE Press, Piscataway, NJ, 1991.
- [2] J. Vanderkooy and S.P. Lipshitz, "Resolution Below the Least Significant Bit in Digital Systems with Dither," *J. Audio Eng. Soc.*, vol. 32, pp. 106-113 (1984 Mar.); correction *ibid.*, p.889 (1984 Nov.).
- [3] A.H. Bowker and G.J. Lieberman, *Engineering Statistics*, Prentice Hall, Englewood Cliffs, NJ, 1972.



# Worth Reading

## TECHNICAL REFERENCE BOOKS

**ADSP-2100 Family User's Manual** is now available in a revised and updated Prentice Hall edition. It is a comprehensive reference for the ADSP-21xx family of 16-bit fixed-point DSP  $\mu$ Ps with varying levels of architectural and code-compatible feature integration. Topics include Base architecture; Integrated on-chip peripherals; System hardware and memory interfacing; Programmer's model and instruction-set reference; and System design and programming examples. 458 pages soft cover. Price \$24. Use book order card, fax or phone the Literature Center.

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## SERIALS

**DSPatch—The DSP Applications Newsletter: Number 30** (16 pages) features EZ Development Tools for the ADSP-2171 fixed-point DSP (EZ-ICE and EZ-LAB) and (p)reviews Analog Devices participation in DSP<sup>x</sup> '94. Also discusses Williams Electronics Games, Inc., DCS (Digital Compression System) CD-quality sound systems for pinball games, such as STAR TREK: THE NEXT GENERATION. Plus regular features: another installment of C Programming for DSP, Q & A, customer workshops (writing programs for PC sound cards based on ADI's Personal Sound Architecture), "Up to Date", new software releases, available literature. Circle 30

## APPLICATION NOTES

**ADM2xxL family for RS-232 communications,** by Matt Smith (AN-375—6 pp.). Circle 31

## IC Accelerometers:

**Using the ADXL50EM accelerometer evaluation module,** by Charles Kitchin, Bob Briano, and Mike Shuster (AN-376—4 pp.) Circle 32

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**Mounting considerations for the ADXL50,** by Mike Shuster and Bob Briano (AN379—2 pp.) Circle 35


**Compensating for the 0 g offset drift of the ADXL50 accelerometer,** by Charles Kitchin and Paul Brokaw (AN380—2 pp.) Circle 36

## ADI AUTHORS IN THE TRADE PRESS

[Reprints not available from Analog Devices]

"Build IF/AGC amp with four parts," by Bob Clarke, Idea for Design in *Electronic Design*, May 30, 1994.

"Autocalibrator nulls dc offsets," by Douglas Mercer and Steve Ruscak, Design Idea in *EDN*, June 9, 1994.

"Locate your amplifier's IMD," by Walt Kester, *Test & Measurement World*, May, 1994. 

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**ERRATA** ••• Analog Dialogue 28-1, p. 16, Fig. 6, horizontal scale calibration omitted. Log scale goes from 20 Hz to 200 kHz, with major divisions from 100 Hz to 100 kHz ••• AD1847 data sheet, Rev. 0, page 28, the 44-lead TQFP package dimensions are incorrect. Until new data sheet available, ask for AD8147 Errata, dated 3/14/94 ••• AD7875TQ and AD7876TQ guarantee 12-bit no-missing-codes, but differential nonlinearity min/max specs are  $-1/+1.5$  LSB (formerly  $\pm 1$  LSB).

**NEW DATA SHEETS** ••• A new data sheet (Rev. B) is available for the AD1856 16-bit PCM Audio DAC; changes include a corrected R-16 SOIC package outline dimension Circle 41 ••• AD7578 ADC has a new data sheet (Rev. B), and AD7582 ADC has a new data sheet (Rev. C); both show an improvement in conversion time with internal clock, to 50  $\mu$ s min/100  $\mu$ s max (from 100/150) Circle 42 ••• An AD1849K data sheet (Rev. 0) is now available for this improved serial-port 16-bit SoundPort® Stereo Codec Circle 43 ••• A new (Rev. A) data sheet is now available for ADSP-21msp50A/55A/56A mixed signal processors Circle 44.

**PRODUCT NOTES** ••• AD420-EB is an evaluation board that demonstrates the various operating modes of our AD420 16-bit digital-to-current-loop converter for industrial control (see page 10). Get in touch with the local Analog Devices sales office ••• The AD7008/PCB is a fully functional evaluation board for the AD7008 Direct Digital Synthesizer modulator, including a 50-MHz crystal oscillator and Windows™ and DOS control software (written in C). Circle 45 ••• The production version of G21, the implementation of a GNU ANSI C compiler for the ADSP-21xx family, is featured in reduced-price ADSP-21xx Family Development Software Release 5.01. Phone (617) 461-3881 ••• **FREE UPGRADE:** 0 to 70°C H-grade versions of DAC8012/8043/8212/8221/8408 are replaced by  $-40$  to  $+85^\circ$  C F-grade versions at no extra cost (slight extra cost for DAC8222FP/8248FP).

**MILITARY AND STANDARDS** ••• The AD871 12-bit, 5-MSPS ADC is available in a /883B version, packaged in 28-lead side-brazed and 44-pin LCC packages. It is also available as SMD 5962-94686. Circle 46 ••• 1994 Military/Aerospace Reference Manual: an errata sheet is available for ADSP-21xx products. Phone (617) 461-3881 ••• The AD780 precision 2.5-V reference is available in a /883B version and as SMD 5962-94636; the AD660 16-bit serial/byte DACPORT® is available in a /883B version and as SMD 5962-94633. Circle 47 ••• Analog Devices has received transitional certification to MIL-I-38535 Qualified Manufacturing Line (QML) status at major manufacturing sites in Wilmington MA and the Philippines. Phone (617) 937-2685.

**SHOWS** ••• Current plans call for Analog Devices to be in the following shows during late 1994. If you're in the neighborhood, come see us ••• Sensors Expo '94, Cleveland OH, 20-22 September ••• DSPWorld '94, Dallas TX, 17-21 October ••• GOMAC '94, San Diego CA, 7-10 November ••• Comdex Fall '94, Las Vegas NV, 14-18 November.

**PATENTS** ••• 5,283,515 to Edward P. Jordan for Automatic calibration system for a ramp voltage generator ••• 5,284,047 to A. Paul Brokaw for Multiplexed single-channel knock sensor signal conditioner system for internal combustion engine ••• 5,289,113 to Richard A. Meaney and Raymond J. Speer for PROM for integrated circuit identification and testing ••• 5,291,122 to Jonathan M. Audy for Bandgap voltage reference circuit and method with low TCR resistor in parallel with high TCR and in series with low TCR portions of tail resistor ••• 5,295,158 to Edward P. Jordan for Dynamically selectable multimode pulsewidth modulation system ••• 5,298,811 to Barrie Gilbert for Synchronous logarithmic amplifier ••• 5,301,295 to Kevin W. Leary and James D. Donahue for Data processor apparatus and method with selective caching of instructions ••• 5,302,848 to Jerome F. Lapham and Brad W. Scharf for Integrated circuit with complementary junction-isolated bipolar transistors ••• 5,311,181 to Paul F. Ferguson, Jr., Apparajan Ganesan, and Robert W. Adams for Sigma delta modulator ••• 5,314,572 to Theresa A. Core and Roger T. Howe for Method for fabricating microstructures ••• 5,314,837 to Herbert J. Barber and Pamela A. Mayernik for Method of making a registration mark on a semiconductor ••• 5,317,199 to Edward P. Jordan for Ramp generator system ••• 5,319,227 to Jerome F. Lapham and Adrian P. Brokaw for Low-leakage JFET having increased top gate doping concentration ••• 5,319,371 to Michael G. Curtin and Michael Byrne for D/A converter with means to prevent output signal instability.

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## IN THE LAST ISSUE

Volume 28, Number 1, 1994, 32 Pages

For a copy, circle 35.

Editor's Notes, Authors

Dual set-point single-chip temperature controller (TMP01)

Intelligent digitizing signal conditioner IC for sensors (AD1B60)

IC vector processor for motor control (AD2S100)

Asynchronous sample-rate converters (AD1890/91)

Microprocessor supervisory ICs spec'd for industrial & MIL (ADM690-699)

Getting the most from IC voltage references

New-Product Briefs:

What's new in Analog & Digital Signal Processing, Communications

What's new in A/D and D/A conversion

What's new in Amplifiers

What's new in Interface Chips, Analog Switches, Signal Conditioning

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